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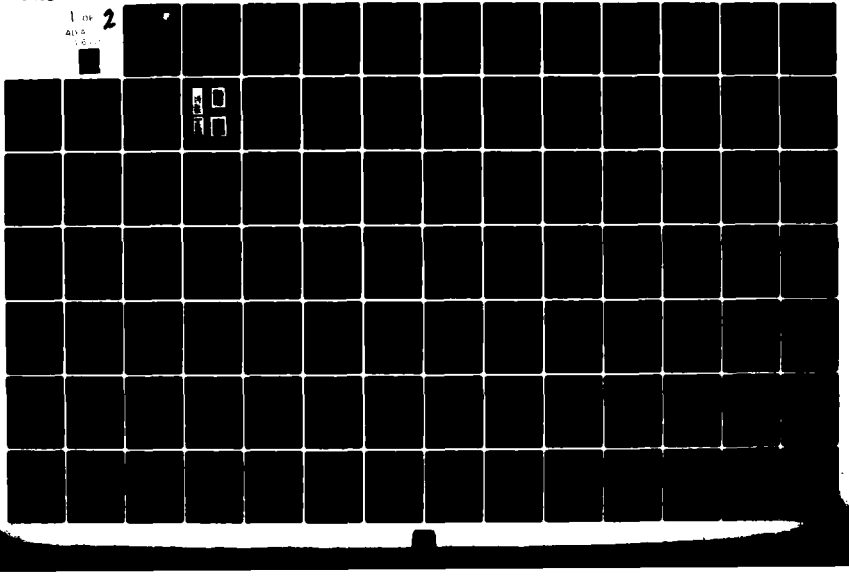

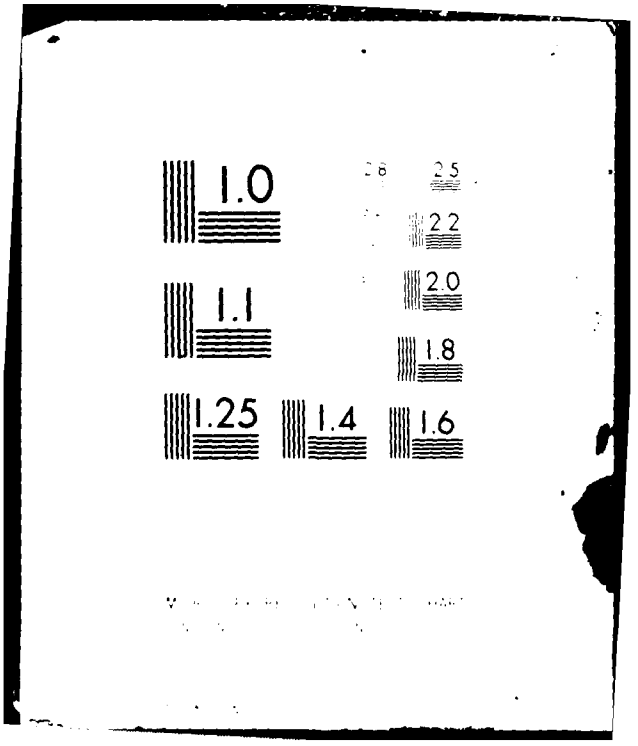
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RADC-TR-82-40
Final Technical Report
March 1982

# ELECTRICAL CHARACTERIZATION OF 16K STATIC RAMS

General Electric Ordnance Systems

James B. Schwehr
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Daniel W. Mui





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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Bench and automatic techniques are used to characterize the performance of several 16K static RAM types. A binary search method is used in conjunction with an array driven program to determine the operating limits of the AC parameters. For comparison, access time measurements are made using a variety of n2 and shorter test patterns. Several device anomalies are discussed.

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CONTENTS

CONTENTS

## LIST OF FIGURES

LIST OF FIGURES
-continued-

## LIST OF TABLES

## Terms and Abbreviations

| | | |
|---|---|---|
| $\overline{CE}$ | - | Chip Enable Signal |
| $C_i$ | - | Input Capacitance |
| $C_o$ | - | Output Capacitance |
| DUT | - | Device Under Test |
| I/O | - | Single Input/Output Pin |
| $I_{IL}$ | - | Input Current Leakage Low |
| $I_{IH}$ | - | Input Current Leakage High |
| $I_{OLZ}$ | - | Output Current Leakage Low |
| $I_{OHZ}$ | - | Output Current Leakage High |
| $I_{CC}$ | - | Device Supply Current |
| $I_{CC1}$ | - | Device Supply Current - Read Mode |
| $I_{CC2}$ | - | Device Supply Current - Write Mode |
| $I_{CC3}$ | - | Device Supply Current - Standby Mode |
| JEDEC | - | Joint Electron Device Engineering Council |
| LSI | - | Large Scale Integration |
| NMOS | - | N-Channel - Metal Oxide Semiconductor |
| SRAM | - | Static Random Access Memory |
| SCA | - | Socket Card Assembly |
| TAVQV | - | Address Valid to Output Valid (Address Access Time) |
| TELQV | - | Chip Enable Low to Output Valid (Enable Access Time) |
| TOLQV | - | Output Enable Low to Output Valid (Output Enable Access Time) |

| | | |
|---|---|---|
| TWLWH | - | Write Low to Write High (Write Pulse Width) |
| TAVWL | - | Address Valid to Write Low (Address Setup Time) |
| TELWH | - | Enable Low to Write High (Enable Setup Time) |
| TDVWH | - | Data Valid to Write High (Data Setup Time) |
| TWHAX | - | Write High to Address Invalid (Address Hold Time) |
| TWHDX | - | Write High to Data Invalid (Data Hold Time) |
| TAXQX | - | Address Invalid to Output Invalid |
| $V_{OL}$ | - | Output Voltage Low |
| $V_{OH}$ | - | Output Voltage High |
| $V_{IH}$ | - | Input Voltage High |
| $V_{IL}$ | - | Input Voltage Low |
| $V_{CC}$ | - | Device Power Supply Voltage |
| $\overline{WE}$ | - | Write Enable Signal |

## EVALUATION

The objective of this study was to establish effective reliability screening procedures for the electrical test and qualification of 16K Static Random Access Memories (RAMs) with special emphasis placed on evaluating existing pattern sensitivity tests. In order to determine the optimum type, number, and sequence of tests which would need to be performed, devices in both 2K x 8 and 16K x 1 configurations and from both Japanese and domestic vendors were evaluated. The 2K x 8 organized memories, aimed at microprocessor oriented systems, are pinout compatible with PROMs and ROMs to allow easy upgrade from RAM to PROM to ROM in system developments.

It was determined that by using a MARCH pattern in place of a GALPAT pattern, a test time reduction of 60% could be achieved without any sacrifice in effectiveness. This is primarily due to designs which disable the decoders before changing addresses.

As a result of this study, MIL-M-38510 detail specifications (slash sheets) were prepared to describe the screening and testing procedures for the 16K x 1 (M38510/291) and the 2K x 8 (M38510/290) devices. These documents describe the electrical characteristics of the devices over specified environmental conditions through the use of /290 and /291, military system designers will have the ability to use state-of-the-art static memories with known parameters and known test requirements.

James J. Dobson

JAMES J. DOBSON

Project Engineer

# 1. INTRODUCTION

## 1.1 Objective

The major objective of this effort is to electrically characterize 16K static random access memories (SRAM) and develop preliminary MIL-M-38510 slash sheets for those devices. In general, the effort involves:

a. Memory market survey to determine production status.
b. Selection and procurement of candidate device types for characterization.
c. Development of test procedures, compatible with automatic test systems.
d. Verification of limits and test circuits via device characterization.
e. Assessment of interchangeability among devices from different manufacturers.
f. Development of preliminary slash sheets based on device analysis and vendor comments.

The development of test procedures includes test pattern sensitivity testing to determine optimum patterns that require short test times but have an effectiveness equal or nearly equal to the much longer $n^2$ type patterns.

## 1.2 Background

The vendor survey performed during the test development phase of the contract, identified four static RAM types as potential candidates for MIL-M-38510 detail specifications. Preliminary slash sheets on these four types were eventually developed and submitted to RADC.

Two of the four vendors could not deliver devices for characterization, either due to design or to production difficulties. Commercial grade devices were procured from the two remaining vendors and characterized. In addition, a few parts were received from a Japanese vendor and from a new domestic producer. Neither of these vendors had near term plans for domestically producing qualified military parts. Nonetheless, the devices were characterized to provide a broader view of the general 16K RAM technology. Table 1.1 summarizes the quantities received, part numbers and the configurations of devices received from all vendors. All types are NMOS.

Table 1.1 Configuration and Quantities of Devices Received from Each Vendor

| | | Part # | Qty. | Config. |
|---|---|---|---|---|
| Vendor A | Mostek | 4802 | 25 | 2KX8 |
| B | TI | 4016 | 22 | 2KX8 |
| C | Inmos | 1400 | 4 | 16KX1 |
| D | OKI | 2128 | 2 | 2KX8 |

A short time after the characterization data was accumulated, both Vendor A and Vendor B indicated that their parts were undergoing major redesigns. Vendor C has indicated that they were accelerating plans for military qualification of their facility and that military devices would be available soon after this report is completed.

A follow-on contract effort will include:

1. Procurement and characterization of military grade parts from the three domestic vendors.

2. Evaluation of all other potential military sources of 16K RAMs.

3. Completion of the preliminary slash sheets and, if necessary, development of new slash sheets to incorporate all appropriate device types.

## 2. DESCRIPTION OF DEVICE TYPES

### 2.1 General Aspects of 16K Static RAMs

Two RAM configurations have been represented by the devices available for the characterization - 2Kx8 and 16Kx1. Some vendors had also indicated the possibility of a 4Kx4 configuration, but none were yet on the market when this report was being written. The x8 or bytewide configuration is intended primarily for byte oriented microprocessor systems, whereas the x1 organization is designed for use by mainframe computers that use large quantities of devices to make memories of a variety of bit widths.

The bytewide concept has also been applied to ROM and EPROM devices, and therefore the impetus was there for JEDEC to make all three types, ROM, RAM, and EPROM as pin-compatible as possible. This compatibility provides flexibility in system development and allows some standardization of memory boards used for ROM, RAM or EPROM devices. The JEDEC 2Kx8 RAM pinout used by Vendors A, B and D is illustrated in Figure 2.1. The 16Kx1 pinout used by Vendor C is shown in Figure 2.2. This pinout provides compatibility with most 4Kx1 static RAMs.

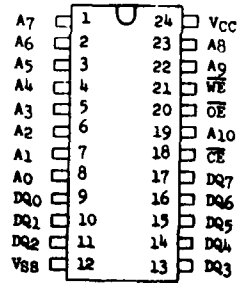



Figure 2.1 2Kx8 Static RAM Pinout

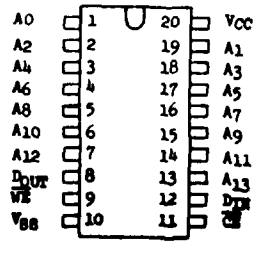
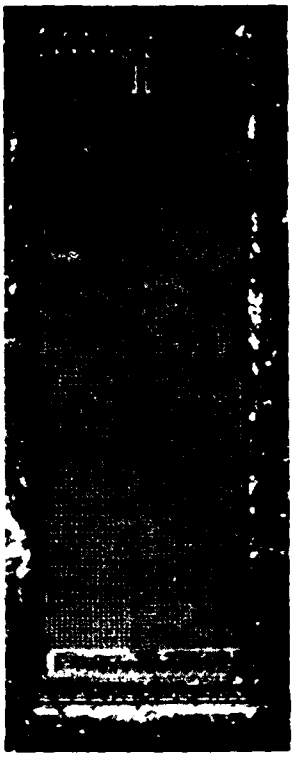
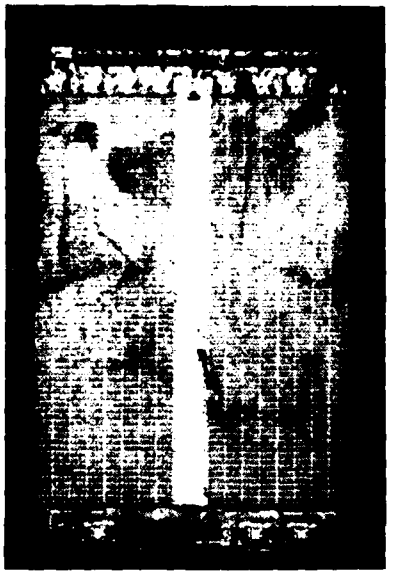



Figure 2.2 16Kx1 Static RAM Pinout

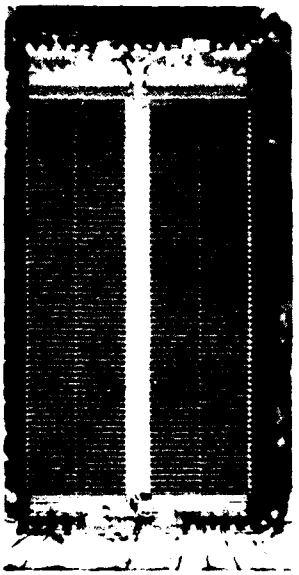
Photographs of a chip from each vendor are in Figure 2.3. All four photographs are to the same scale so that a visual size comparison can be made. Actual chip dimensions and cell sizes are listed in Table 2.1.



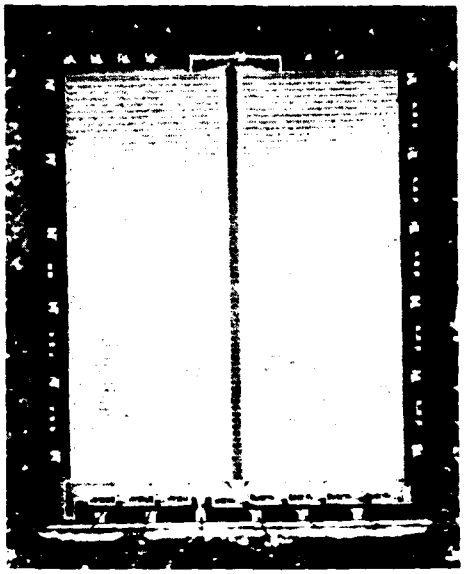
Vendor A - 4802



Vendor B - 4016



Vendor C - 1400



Vendor D - 2128

Figure 2.3 Chip Optical Micrographs (11.6X)

Table 2.1 16K RAM Chip Dimensions

| Vendor | Length (mil) | Width (mil) | Area ($mil^2$) | Cell Size ($mil^2$) |
|---|---|---|---|---|
| A | 331.2 | 107.2 | 35510 | 1.3 |
| B | 251.5 | 161.4 | 40590 | 1.5 |
| C | 251.5 | 120.3 | 30250 | 1.07 |
| D | 237.3 | 191.7 | 45490 | 1.89 |

All four types use a four transistor cell with polysilicon pull-up resistors. A schematic example of this type of cell is illustrated in Figure 2.4.

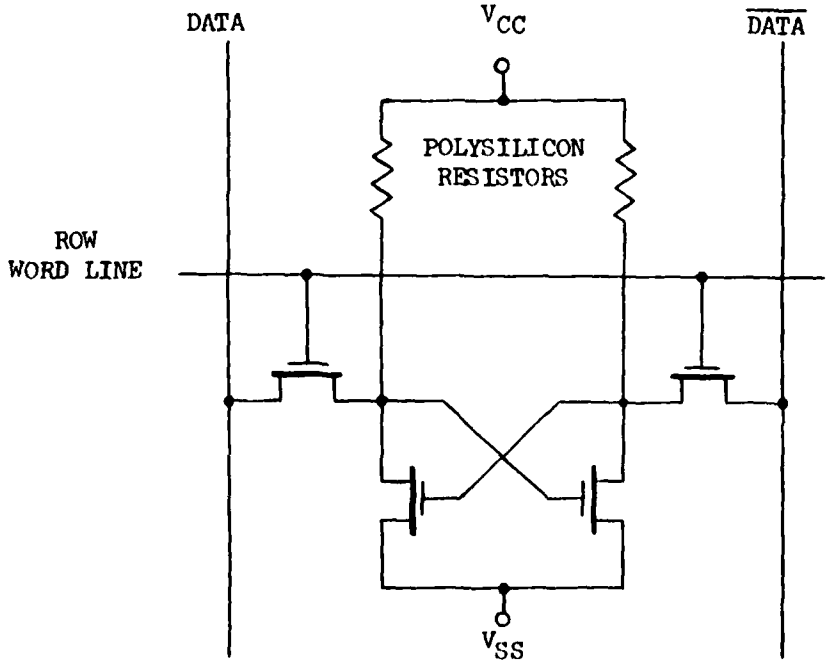



Figure 2.4 Static RAM Cell With Polysilicon Pull-ups

All four device types also use substrate bias generators to reduce the body effect of the substrate.

The following paragraphs briefly describe some specific aspects of each.

## 2.2 Aspects of Specific Device Types

### 2.2.1 Vendor A

This 2Kx8 device is basically made up of two of its 1Kx8 predecessors placed end-to-end giving it the unusual aspect ratio illustrated by Figure 2.3. The bit lines which run lengthwise are metal. Thus the propagation delay to the sense amp from a cell at the opposite end of the column is nearly the same as from a cell near the sense amp. However, charge times are increased since the higher capacitance of the extra long lines must be charged through the high resistance pullup of the memory cell currently driving the bit line. The vendor uses very high resistance pullups to reduce static power consumption.

To gain speed Vendor A's device is equipped with dynamic peripheral circuitry. During a READ cycle, a logic transition at any one of the address inputs is sensed by a transition detector that in turn initiates a clock that controls the row address decoder and the sense amps. The address lines can be changed at any time to initiate a new READ cycle. A READ operation appears fully asynchronous to the user.

During a WRITE cycle on the other hand, the states of the address inputs are latched when $\overline{WE}$ and $\overline{CE}$ are both low. As $\overline{WE}$ or $\overline{CE}$ goes back to a logic high the actual WRITE operation is performed. A delay time later, an internal clock terminates the write cycle and the device is available for a new cycle.

When the internal dynamic circuitry is clocked, supply current spikes of up to 150mA are caused. Good grounding techniques are required when using this part. As will be discussed in Section 3.3, a special Tektronix test adapter was built to reduce the ground noise generated by this device type during testing.

### 2.2.2 Vendor B

Few details on the design of Vendor B's device were available. Nonetheless, some observations can be drawn from their device specification, general chip layout and actual measurements.

This device is probably the most conservatively designed of the three domestic types. It has the largest cell and chip size of these

three vendors. Since the long row select lines are non-metalic, their resistances are a significant factor in determining access times. It could not be determined if the device contained any special circuitry to overcome the delaying effects of the long row select lines. However, longer access times (as compared to the other two vendors) suggests that special precharge or precondition circuits are not utilized.

The vendor has indicated that a redesign of the device is underway to obtain better performance at the military temperature extremes.

### 2.2.3 Vendor C

The device from Vendor C is the only one of the four types that is configured as a 16Kx1. It is also the only device that implements a low power standby mode when deselected.

This part functions externally as an asynchronous device although an internal pulse is generated by an address edge. Geometries are somewhat conservative, but several unique circuit techniques are used to achieve short access times. A logic transition on any one of the row address inputs initiates an internal pulse that supplies a pull-up voltage to the previously undriven bit lines and precharges them to a voltage between those of a 1 and a 0. This operation is being performed as the address decoders are selecting a row of cells. When the cells are finally selected, the bit lines are already part way to the next logic state. A selected cell thus requires less time to drive the bit lines to the full voltage required for sensing.

A bootstrap circuit, is used to supply a higher than $V_{CC}$ level to the column select gates. This is intended to optimize channel on resistance. It also permits the use of transistors whose thresholds are well above zero and therefore, not susceptible to turn on with increased temperature or with slight upward shifts in substrate bias voltage.

Vendor literature indicates that this device type has two spare columns which can be selected through proper wafer level programming of polysilicon fuses. An inspection of the chip shown in Figure 2.3 using high magnification optical microscope revealed several polysilicon fuses, one of which had been blown. Since a fuse had been programmed, it was assumed that at least one of the spare columns had been used. A spare column is located on the inside edge of each half of the memory matrix.

### 2.2.4 Vendor D

As indicated earlier, this vendor was non-domestic and has no present plans for domestic production of parts. Two parts were received as samples and were evaluated to obtain a general assessment of the

technological expertise used in the design.

Although the chip from Vendor D is significantly wider than the domestic types, the area covered by active circuitry is only slightly larger than that used by Vendor B. As one might expect, actual data shows that Vendor D's device is a little slower than Vendor B's. The clearance afforded the I/O pads from the rest of the circuitry is substantially more than on the domestic chips. The location of pads on the sides of the memory array is rather unusual since long parallel runs are needed to route the I/O signals down to the ends of the array where the interface circuitry is located.

## 3. DEVELOPMENT OF AUTOMATIC AND BENCH TESTS

### 3.1 Automatic Test Equipment

The test equipment used to characterize the 16K RAM types is a Tektronix S-3270 Automatic Test System. The system contains an 1804 test table capable of interfacing 64 input and 64 output pins. Among the system options is the R2942 Programmable Pattern Generator which generates test patterns from algorithms. Included in the R2942 is the CL-10T topological feature, which is used to counteract the "scrambled" address decoding internal to the memory under test. By this means, known physical locations within the memory matrix can be easily accessed in a specific sequence.

Other system capabilities include:

a. 14 programmable clock phases (10 drive, 4 compare) with 1ns resolution

b. functional testing at speeds up to 20MHz

c. DC measurement:force V, measure I; force I, measure V

d. device under test temperature control from -60° to 160°C

e. data logging and reduction

f. computer graphics display

To interface the device under test (DUT) to the test system, a socket card assembly(SCA) is used to electrically connect DUT pins to specific 1804 test table pins. Many memory test patterns used during the 16K RAM effort require separation of DUT row address pins from column address pins. Therefore the SCA must connect each row address pin to one of a specific group of 1804 test table pins and each column address pin to one of a different group of 1804 pins. Even though two domestic 16K RAMs had the same number of address pins, they were not identical in their assignment of the address pin functions (ie as a row or as a column pin). This required each type to have its own SCA. Additional discussion on the SCAs is provided in section 3.3.

## 3.2 DC Test Development

### 3.2.1 Standard Programming Guidelines

General Electric Ordnance Systems has developed standard programming guidelines for use with the Tektronix test system. The guidelines are basically well structured independent blocks of test software. Each block contains the statements that initialize the test system, call for DUT power and perform a specific type of test such as an input current or output voltage measurement. A user can build a device test by selecting the appropriate blocks and arranging them in any desired sequence. The user must incorporate information about the device such as pin assignments, voltage/current test conditions, and pass/fail test limits.

These standard guidelines have several significant time saving advantages:

a. simplified test generation

b. minimized test debug effort

c. ease of test program maintenance, even by personnel not involved in the original development

The guidelines consist mainly of blocks for measuring DC parameters, but as other parameter measurement techniques are developed, they are considered for use as "standard" techniques and added to the guidelines if appropriate.

The standard guidelines were utilized to develop the 16K RAM DC characterization software for each device type. Minimal changes were made to provide automatic temperature control, data logging and vendor-specified voltage and current test conditions and limits. In addition, capability was added to allow a supply current measurement while the DUT was being cycled through READ and WRITE operations.

### 3.2.2 Parameters and Test Conditions

The DC characterization measured the following parameters at -55°, 0°, 25°, 70° and 125°C:

Input/output leakage current ($I_{IL}$, $I_{IH}$, $I_{OLZ}$ & $I_{OHZ}$)

Output logic high voltage ($V_{OH}$)

Output logic low voltage ($V_{OL}$)

Supply current - READ mode ($I_{CC1}$), WRITE mode ($I_{CC2}$), standby ($I_{CC3}$).

3.2.2.1 Leakage Current

a. Input Leakage Current ($I_{IL}$, $I_{IH}$)

The leakage current of each input terminal was measured with $V_{IN}$ at 0.4 and at 2.4V. When non-data pins were measured, all other pins were driven to 2.4V. When bidirectional data pins were measured $\overline{CE}$ and $\overline{WE}$ were driven to 0.4V; all other pins remained at 2.4V.

b. Output Leakage Current ($I_{OLZ}$, $I_{OHZ}$)

The leakage current of each data output terminal was measured while externally applying 0.4V, then 2.4V. All input and bidirectional terminals (except the output selected for measurement) were set to 2.4V.

3.2.2.2 Logic Output Voltage

a. Logic High Output Voltage ($V_{OH}$)

The voltage at each output was measured while the output was in the logic one state and sourcing the vendor's maximum specified current. $V_{CC}$ was set to 4.5V.

b. Logic Low Output Voltage ($V_{OL}$)

The voltage at each output was measured while the output was in the logic zero state and sinking the vendor's maximum specified current. $V_{CC}$ was set to 4.5V.

3.2.2.3 Supply Current ($I_{CC}$)

A supply current measurement was made while the device was in each of three operating modes - READ, WRITE and standby (chip deselected). The

READ and WRITE modes involved continuous memory cycling to insure that the maximum average supply current of dynamic circuitry was included in the measurement. In all three modes $V_{CC}$ = 5.5V, $V_{IL}$ = 0.4V, $V_{IH}$ = 2.4V and the data output pins were connected to the AC load described in section 3.3.2.

a. READ Mode

The device was preconditioned by writing a zero at address 0 and a one at the maximum address. While the supply current ($I_{CC1}$) measurement was performed, $\overline{OE}$ was set to $V_{IL}$, $\overline{WE}$ to $V_{IH}$, and all address inputs were continuously toggled between a zero and a one to simulate a READ at the minimum and maximum locations.

b. WRITE Mode

$\overline{CS}$ was set to $V_{IL}$, and $\overline{OE}$ to $V_{IH}$. While the supply current ($I_{CC2}$) measurement was performed $\overline{WE}$, the data inputs and the address inputs were continuously toggled. The timing parameters were set to properly satisfy the WRITE cycle conditions.

c. Standby (Deselect) Mode

All input terminals were set to $V_{IH}$ while supply current ($I_{CC3}$) was measured. Although only one device type had an actual standby mode, all devices were subjected to this test.

## 3.3 AC Test Development

### 3.3.1 General Characterization Goals

The general philosophy behind the development of AC-functional characterization capability included several design goals relating to overall test effectiveness. That is, the characterization should verify or establish:

a. $V_{OH}$ and $V_{OL}$ limits under dynamic maximum load conditions

b. $V_{IH}$ and $V_{IL}$ dynamic operating limits

c. operating time limits

d. functional integrity

e. performance over the -55° to 125°C temperature and the 4.5 to 5.5V $V_{CC}$ limits.

During the characterization of a particular timing parameter, all other parameters are set to vendor specified limits or to less stringent values. This criteria guarantees that as the selected parameter is adjusted toward its operating limit, a failure is due to that parameter. The philosophies behind the selection of device loads and test patterns are discussed in more detail in the following sections.

### 3.3.2 Hardware

#### 3.3.2.2 Tektronix Socket Adapters

Three Tektronix socket card adapters were built, one for each vendor, based on that vendors assignment of row and column address pins. The 16KX1 adapter was intended for use with devices from a vendor who was unable to deliver parts in time for characterization. This adapter was used to evaluate the four devices from Vendor C.

During initial tests, access time measurements of Vendor A parts were not repeatable. Investigation revealed large voltage spikes on $V_{CC}$ and ground pins. Since the device used clocked peripheral circuitry, current spikes of up to 150mA occurred during device cycling. More decoupling capacitance substantially reduced $V_{CC}$ noise but had little effect on the ground noise spikes which sometimes reached 1V in amplitude (measured between DUT ground and test table ground). The solution to the ground noise problem was found in a new adapter design using a ground plane that connected to 64 test table contact points equally spaced around the circumference of the socket card. The original adapter had used a braided wire with a single connection point to the 1804 test table. The new adapter reduced the 1V spikes to less than 100mV. It resulted in consistent data and provided a much more favorable and accurate picture of the performance of Vendor A's parts.

#### 3.3.2.3 Output Loads

Since each vendor guarantees that his device will meet its $V_{OH}$ and $V_{OL}$ specifications, the output loads used during AC testing are designed to provide maximum specified current loading at these voltages. Figure 3.1 illustrates an output load. Resistor $R_L$ was selected to provide the maximum

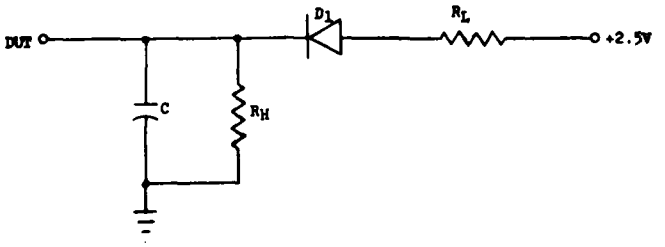



Figure 3.1 Output Load Circuit

load current at the maximum allowed output logic low voltage. $R_H$ will provide maximum load current at the minimum allowed logic high voltage. The 50pF capacitance includes the parasitic capacitance of the test equipment.

To verify that the outputs reach their specified voltage limits, in an AC environment, the test system detection thresholds were set to those voltage limit values.

### 3.3.3 Software

#### 3.3.3.1 Parameter Arrays

In order to provide a standard S-3270 AC test which could be used for different 16K RAM types, an array driven test was developed. An array containing all necessary timing conditions based on vendor specifications was developed for each device type to be characterized. The test program accesses the appropriate array for the timing information to be applied during the functional tests. Additional 16K RAMs can be added to the current test capability by reviewing the vendor's specification and creating a new timing array. An example of an array is in Figure 3.2. Each row in the array contains the timing information and test routines applied during the characterization of one AC parameter. The first column contains mnemonics that identify the parameter associated with each row. In addition to timing conditions, the array specifies logic levels to be applied during testing.

#### 3.3.3.2 Binary Search

A classical technique for characterizing an AC parameter involves incrementally adjusting the parameter through a predetermined range and recording a test pattern pass/fail response at each parameter setting. A plot of the responses versus magnitude of the parameter will exhibit the operating limit (pass/fail boundary) but only to the accuracy of the incremental step size. Increased accuracy requires the use of smaller steps, which implies a larger number of test executions. A total of 31 test executions are required if the range is 300ns and the step size is 10ns.

The 16K RAM effort made use of a binary search technique to determine the operating limit of each selected AC parameter. A binary search isolated the parameter pass/fail boundary within a range of values, by repetitively testing the device and eliminating one half of the then current range of values. The half that is eliminated is based on outcome of the test. The half that is retained encompasses the pass/fail boundary.

The initial range of values for a parameter is made sufficiently wide to guarantee that the operating limit (pass/fail boundary) is enclosed. Therefore, the device will fail with the parameter set to one end of the range and is expected to pass with the parameter set at the other end. The value at the "passing" end is equal to the vendor specified limit or to a less stringent value. If a device fails a test at that value, characteri-

```
SAMPLE.ASC:16K
DEVICE      16Kx1  STATIC  RAM      VENDOR  C  TIMING
LOGLEV     2.0V     0.8V   0.0
COM VAP #    DLT :-CYC-:  -WP-    :  -OE-    :   -CS-   :  -DATA- :STR : -ADDRESS- :
TAA     1   100N 1 200N  50N  40N   0N   0N   0N 150N   0N 150N  75N   0N 150N
TCA     2   100N 2 200N  50N  40N   0N   0N  20N 130N   0N 150N  75N   0N 150N
TCZ     4   100N 2 200N  50N  40N   0N   0N   0N  90N   0N 150N  75N   0N 150N
TWP     6   100N 2 200N  50N  40N   0N   0N   0N 150N   0N 150N  75N   0N 150N
TAS     7   150N 2 200N  50N  40N   0N   0N   0N 150N   0N 150N 125N  20N 130N
TCS     8   150N 2 200N  50N  40N   0N   0N  35N 120N   0N 150N 130N   0N 150N
TDS     9   100N 2 200N  50N  40N   0N   0N   0N 150N  40N 110N 130N   0N 150N
TAH    10   100N 2 200N  80N  40N   0N   0N   0N 150N   0N 150N  75N   0N 150N
TDH    11   100N 2 200N  80N  40N   0N   0N   0N 150N   0N 130N  75N   0N 150N
TCH    12   100N 2 200N  80N  40N   0N   0N   0N 130N   0N 150N  75N   0N 150N
TCD    13   -50N 3 400N 200N  40N   0N   0N   0N 130N   0N 375N  75N   0N 375N
TAD    15   100N 2 200N  50N  40N   0N   0N   0N 175N   0N 175N  75N   0N 100N
STOP
END
```

Figure 3.2 Example of Parameter Array

zation of that parameter is terminated.

When a device passes testing with the parameter set at the passing end of the range, the parameter is set to the middle of the range and tested again. A subsequent pass results in the passing end of the range being pulled in to the parameter value. A failure would cause the "failing" end of the range to be pulled in to the parameter value. This process cuts the range size in half. After readjusting the range, the parameter is again set to the middle of the range before the test pattern is again executed. On each repetition of this process, the range is reduced by one half, but the range continues to enclose the operating limit of the parameter. When the range is 1ns wide, the passing end is the desired worst case operating limit.

The number of steps, n, to reduce a range, r, to x ns can be found through the relationship

$$x \cdot 2^n = r \ . \qquad (3.1)$$

Therefore,

$$n = \frac{\ln r/x}{\ln 2} \ . \qquad (3.2)$$

For an r of 300ns and x = 10ns, n would be 4.9. Since n is not an integer, 5 steps would be performed to isolate the value to less than 10ns. This is in sharp contrast to the 31 steps required in the classical approach. A general flowchart of the AC test program including the binary search routine is shown in Figure 3.3.

3.3.3.3 Test Patterns

The AC characterization not only determined the operating limits of the timing parameters but also verified the integrity of the internal functions under dynamic conditions. The internal functions of memory can be divided into the following basic blocks:

a. address decoders

b. sense amps

c. write circuitry

d. memory array

e. data I/O circuitry

Certain functional characteristics and AC timing parameters can be associated with these blocks. Therefore, when an AC parameter is characterized,

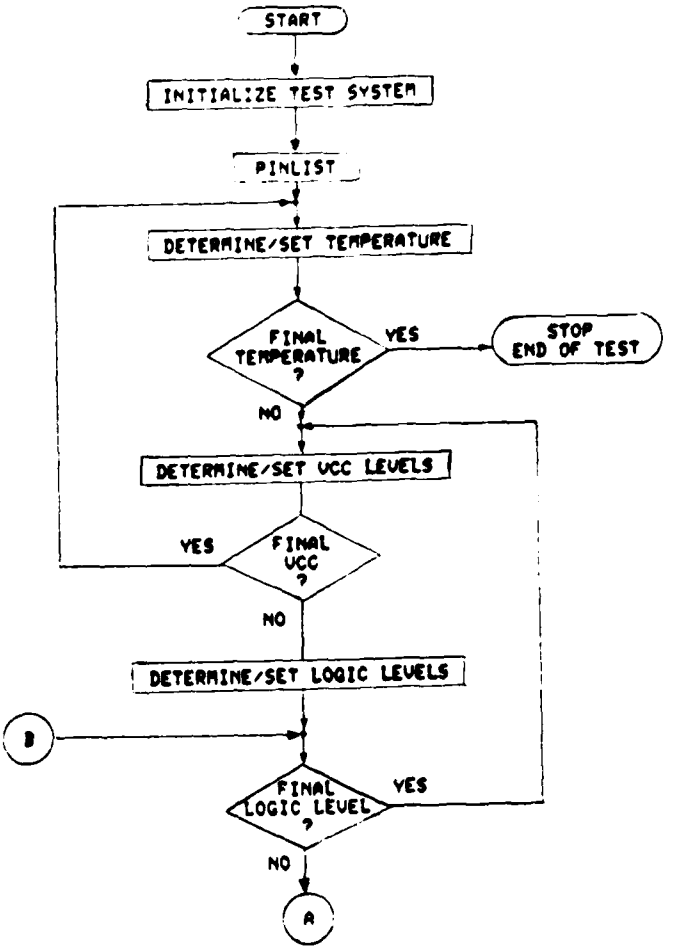



Figure 3.3a AC Parameter Test Routine

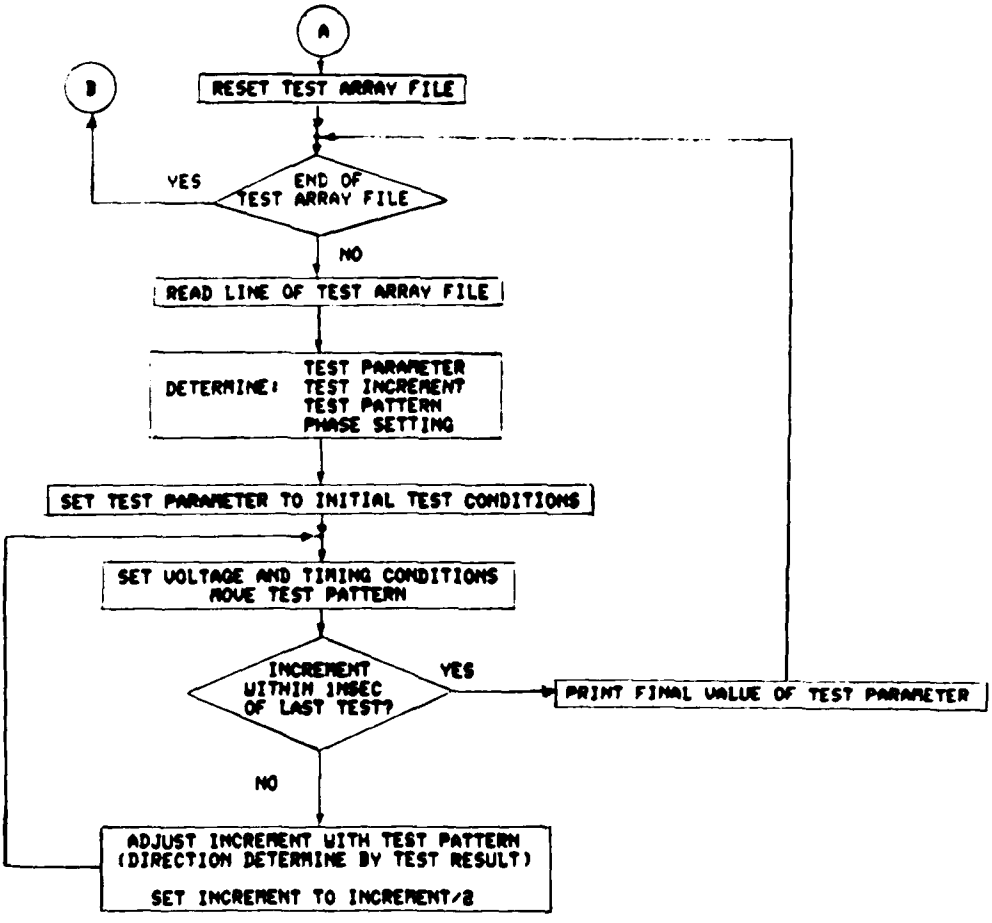



Figure 3.3b AC Parameter Test Routine

a test pattern is selected to provide stringent dynamic functional conditions to the appropriate block.

The address decoder response may best be verified by patterns that maximize the number of internal transitions. An $n^2$ pattern such as Galloping is ideal for this situation. However, characterizations requiring repetitive pattern executions at many temperature and voltage combinations, are very time consuming for large memories. An alternate shorter pattern is desirable. A test pattern sensitivity study performed on devices from each vendor determined that both the March and the Gallop patterns (and several others) provide the same access time characterization results. Therefore, the March pattern was used to characterize the access time of all devices under all temperature and voltage conditions.

An effective test of the sense amp circuits is one that requires the circuits to detect a one followed immediately by a zero and vice versa. A March pattern is good choice for applying these conditions.

The write function utilizes control circuitry to force data and $\overline{\text{data}}$ lines, selected by the column address, to a desired state. The cell intended to receive the data is selected by the row address. An effective test of the write function is one that causes the circuitry to force every data (and $\overline{\text{data}}$) line to a zero, when a cell is driving the line to a one and vice versa. Again a March pattern performs this function.

An effective test of the memory array is one that verifies the independence of each cell from all others. An $n^2$ pattern such as Walking would be unacceptable, and an alternate pattern is necessary.

Inspection of vendor-supplied bit maps reveals that devices with 8 data outputs have 8 internal groups of cells that are physically distinct and separate. Therefore, the bit independence test can be limited to one that verifies independence of one group from adjacent groups and independence of each cell in a group from all other cells in the same group. For the 2KX8 parts, verification of adjacent cell group independence is performed by using a 10101010 data word and its complement during testing. An address uniqueness test not only verifies cell independence within each group in a 2KX8 device, but also completely verifies bit independence in the 16KX1 parts. Bit independence and address uniqueness are equivalent expressions when applied to devices with a single data output. Since a March pattern meets the above requirements, the memory array is thoroughly tested when AC parameters are characterized with that pattern.

The circuit associated with each data input or output must be able to pass a zero and a one independently of any other input or output circuit As with memory array cell groups, the independence of one data input or output pin can be verified by using a 10101010 data word and its complement during testing.

The test patterns used during the AC characterization apply an extremely small set of possible address, read and write sequences to each device. Due to a design or production defect, there may exist an input sequence that causes the device to malfunction. In order to exercise the memory functional blocks through a more extensive set of sequences, many address patterns were applied in a pattern sensitivity study. The study is described in more detail in section 3.4.6.

## 3.4 Other Characteristics

### 3.4.1 Input and Output Capacitance ($C_i$, $C_o$)

Device input and output capacitance measurements were made using a Boonton Model 71A capacitance bridge. This bridge uses a test frequency of 1MHz. The test signal amplitude was set at 50 mVp-p.

During the measurements the device was connected directly to the bridge using short leads to minimize the effect of lead inductance and capacitance.

### 3.4.2 Output Compare Levels

Many of the more recent automatic test systems provide capability to dynamically test memories while using dual output detection thresholds. During the 16K RAM characterization on the Tektronix S-3270, the thresholds were set to the RAM minimum $V_{OH}$ and maximum $V_{OL}$ specified levels of 2.4V and 0.4V. Many vendors including A, C, and D still use the single output reference point of 1.5V for specifying propagation times. A user of a device with 1.5V referenced limits does not know the worst case time for an input change to propagate to the output as a valid one or zero. This unknown time can be significantly longer than the limit specified at 1.5V.

Access time measurements were therefore performed on the S-3270 at various detection thresholds to determine the impact of reference points on access time data. The measurements were performed at 25°C with $V_{CC}$ = 5.0V.

### 3.4.3 Output Disable Time

A prime concern in the design of systems is bus contention. To avoid potential damage to outputs connected to a bus, system timing must be such that each bus line is driven by only one output at a time. The system designer must therefore know how long it takes a device output to respond to the disable and enable input signals.

An output, once enabled, must be able to drive the bus line to a specified logic level. Therefore, the capacitance in a load circuit (reference Figure 3.1), is necessary to simulate worst case loading. Turn on delay is that time required for the output to reach a minimum $V_{OH}$ or maximum $V_{OL}$ level. This parameter is easily measured using the same technique applied to most other AC output parameters such as address access time.

Measurement of output turn off delay is another matter. The voltage at the output pin, at turn off, largely becomes a function of the time constant of the capacitance and the load resistances. The output stage actually turns off long before the voltage on the output pin reaches its stable high impedance level (determined by the load circuit).

A frequently used indicator of the turn off delay is that time between the output disable signal and an output voltage change of 0.5V. It is suspected that this criteria is somewhat arbitrary. Therefore, the turn off delay measurements made during the contract effort concentrated on correlating this output voltage criteria with actual output current, through bench measurements.

While taking measurements the load circuit shown in Figure 3.4 was connected to the output. The circuit is similar to that used during characterization of other AC parameters. Here, also $R_L$ and $R_H$ are selected to provide specified maximum output sink and source currents at maximum $V_{OL}$ and minimum $V_{OH}$ levels. $C_L$ is the capacitive load that includes the parasitic capacitance of the scope probe and test fixture. To determine the effect of load capacitance on output voltage, the turn off delay measurements were performed for three $C_L$ values, 15, 35 and 50pF.

The resistor, $R_S$, in series with the output pin is used to develop a voltage that is proportional to the output current. The resistance is kept as small as possible to minimize its effects on the voltage seen across $C_L$. $R_S$ was 240 ohms when the turn off delay was measured with the output state initially at a one. $R_S$ was 75 ohms when the output was initially at a zero.

Figure 3.4 illustrates the scope probe locations for taking the turn off delay measurements. Also shown are sketches of the resulting waveforms when both probe signals are superimposed on one another using the same vertical gain and zero volt reference.

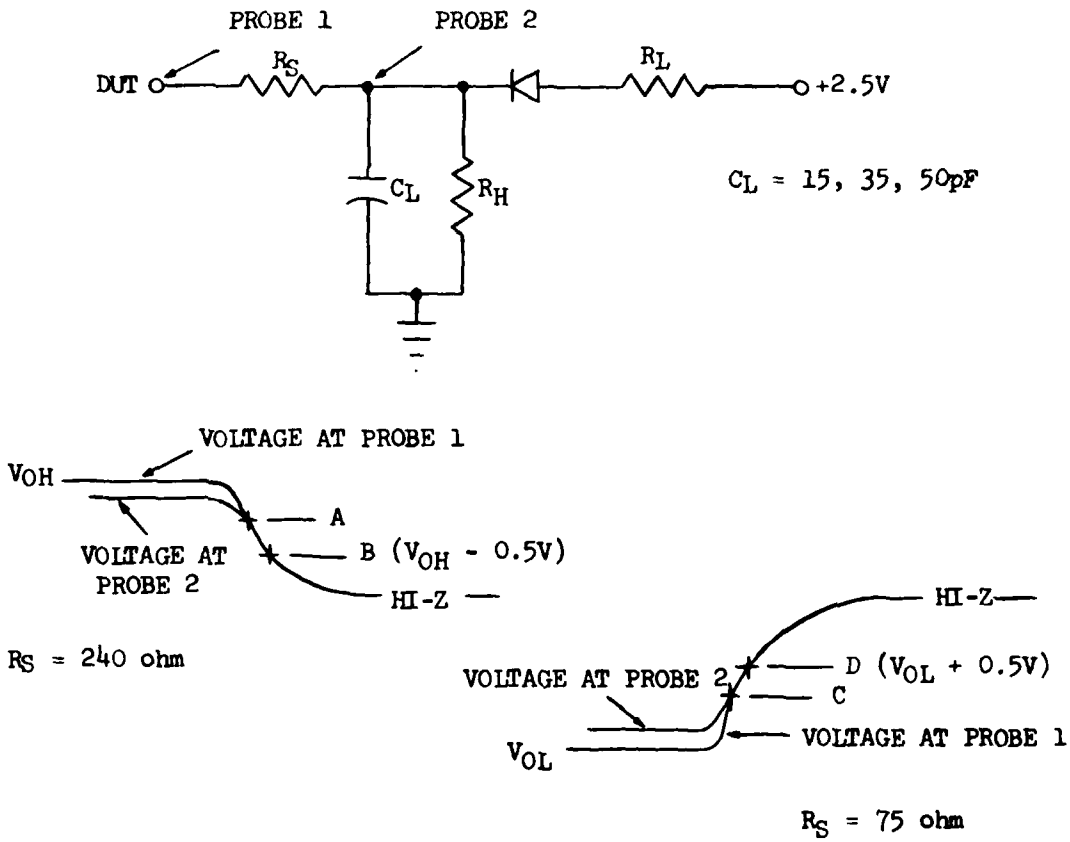



Figure 3.4 Output Load Circuit and Waveforms
for Turn-Off Time Measurements

Since the difference between probe A and probe B voltages indicates that output current is flowing, one can determine the point at which the output current falls to zero. This is the point at which the output is effectively in the high impedance state.

Although the technique of observing the output current via the series resistor voltage was successful, it cannot easily be implemented on an automatic test system. The resistor value is necessarily small to minimize its effects on output voltage. Thus, the voltage drop across the resistor is large enough tc determine whether the output is on or off, but not large enough for an automated, accurately timed amplitude measurement.

It is recommended that future contract work investigate effective methods of measuring output turn off delay that accurately masks the effects of output capacitance, including parasitic capacitance, and safeguards the DUT output from potential damage. The investigation should include techniques already proposed (e.g., that described in RADC-TR-80-263) as well as development of other techniques that can be implemented on automatic test equipment.

### 3.4.4 Input Threshold Voltage

Input threshold measurements were performed on the bench to determine the margin between thresholds and the vendor specified input voltage limits. When measuring the threshold of a particular input, a periodic signal is applied to that pin. For a logic one threshold measurement, the logic zero voltage of the input signal is set at 0.0V. The logic one voltage is then incrementally increased, from a very low voltage ($\simeq$ 0V), until the voltage is reached at which the output responds properly. That voltage is taken as the threshold value. For a logic zero threshold measurement, the logic one voltage is set at 3.0V. The logic one voltage is then incrementally decreased from a high voltage ( $\simeq$ 3.0V) until the proper output response is observed.

Measurements were performed at 25°C on several inputs of devices selected from each vendor. Some data was also taken at -55° and 125°C to determine the effects of temperature.

### 3.4.5 Input Logic Level Sensitivity

Many vendors specify timing parameters at input voltage conditions less stringent than the $V_{IH}$ and $V_{IL}$ limits. The user is left to guess whether or not the specified $V_{IH}$ and $V_{IL}$ limits are adequate for dynamic operating conditions.

To establish the integrity of the $V_{IH}$ and $V_{IL}$ limits specified by the four subject vendors, access time measurements were performed on the S-3270 system at various input voltage conditions. In section 4, the results are discussed and related to the $V_{IH}$ and $V_{IL}$ limits as well as the

threshold measurements.

3.4.6 Pattern Sensitivity

A test pattern sensitivity study was performed on a selected number of devices from each vendor. The study had two objectives: 1) verify RAM logic integrity under a variety of address, read and write sequences, 2) identify shorter patterns that are as effective as $n^2$ patterns in verifying access time limits.

Use of shorter effective test patterns would dramatrically reduce the 16K RAM characterization time. As many as 500 pattern executions are required for each device to determine access time at the various temperature and voltage conditions.

If found, a short, effective test could be specified in the MIL-M-38510 slash sheet. This will reduce test time (and thus cost) of reliable, qualified military devices.

During the pattern sensitivity testing, the input timing conditions were set to optimum values to avoid failures that could mask functional failures or affect access time measurements. Other test conditions were:

a. temperature = 25°C

b. $V_{CC}$ = 5.0V

c. $V_{IH}$ = 3.0V, $V_{IL}$ = 0.4V

d. output detection thresholds = 0.4V and 2.4V

Descriptions and flowcharts of the test patterns used are in the Appendix (section 8).

3.4.7 Staggered Address Test

Vendor A's device uses a transition detector on each address input. According to vendor information, a transition on any one of these inputs will immediately initiate a new read cycle, even if a read cycle is in progress. Ideally then, the last address input to change is the one from which access times can be measured. The staggered address test was designed to verify this condition. It was felt that if one address input was late in switching (skewed) relative to the others, it might have no impact until the read cycle initiated by the other inputs was complete. The test consisted of delaying one address input signal from all others and measuring access time from the skewed signal. Many delay intervals were selected.

Vendor C's device also uses transition detectors to initiate

memory cycles. However, the time schedule did not permit use of the staggered address test on this device type. Lack of data was not deemed critical since the vendor was, at that time, not considered a potential military vendor.

### 3.4.8 Power-up Readiness

A device with a substrate bias generator requires some time after power-up to bring the substrate to a stable negative voltage. Reliable operation may not be possible until this occurs. To characterize the time delay from power-up to reliable operation of the 16K RAMs, two different measurements were performed:

1.) direct measurement of the substrate bias voltage (if accessible externally) versus time from application of the external supply. Supply current was also monitored during this measurement.

2.) measurement of time delay required between power-up and a full memory write that resulted in correct data.

The measurement in item 1 was performed on the bench at 25°C. Item 2 was an automatic test procedure performed on the Tektronix S-3270 at -55°, 25° and 125°C. As will be discussed in section 4, measurements of the substrate bias were also instrumental in evaluating several devices from Vendor B that exhibited AC and DC failures at -55°C.

Time delay measurements, referenced to supply voltage require that the supply rise time be fast relative to the magnitude of the delay time. In addition, the switching of the supply voltage must be accurately controlled so that a repetitive power on/off cycling can be obtained for scope or automatic test system triggering. The bench power supplies and those within the Tektronix S-3270 require at least a few milliseconds to reach the desired level and thus are too slow. The S-3270 sector drivers could be controlled accurately timewise but cannot source the required supply currents. To provide the required supply voltage timing and current requirements, power supply switching circuits were developed.

#### 3.4.9.1 Bench Test Circuit

Figure 3.5 illustrates the switching circuit successfully employed for bench measurement of the substrate bias stabilization time. The amplitude of the positive going pulse, F, from the clock generator is adjusted to $V_{CC}$ + two diode drops to provide the desired pulsed $V_{CC}$ level at the device under test (DUT). Diode D1 merely furnishes reverse bias protection against an inadvertent feedthrough from the +10V circuit supply. $R_3$ pulls the transistor base to ground when the input pulse goes to 0 volts. $C_1$ is placed as close as possible to the transistor collector to provide optimum

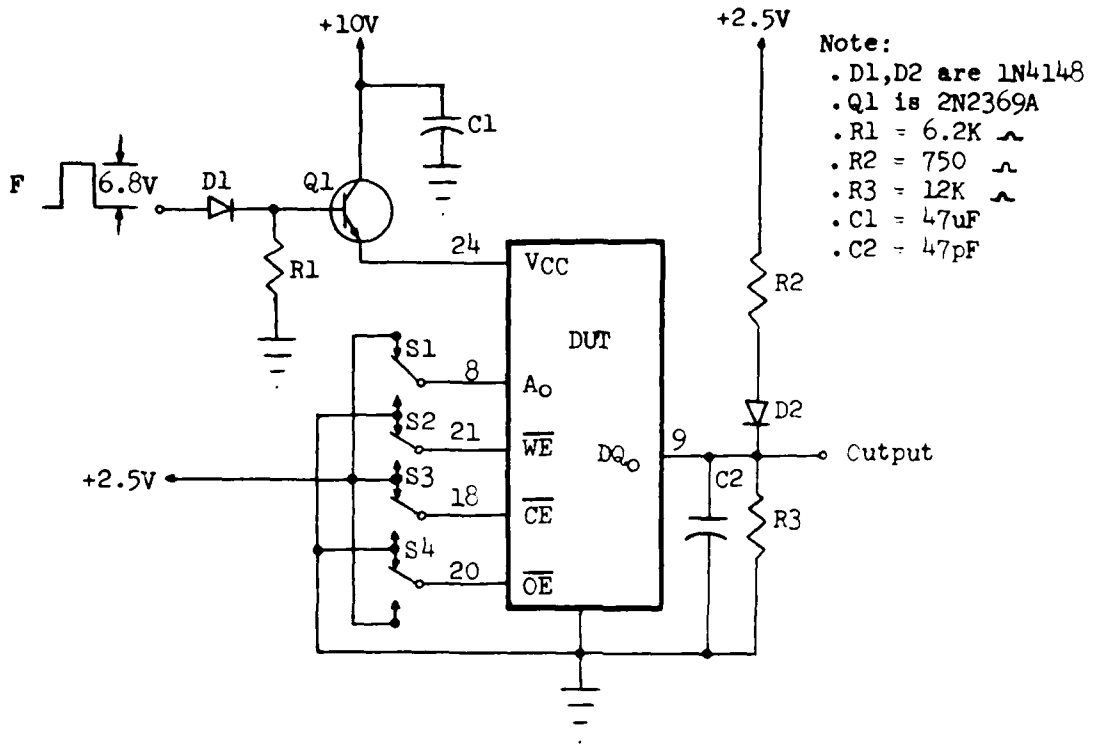



Figure 3.5 Supply Switching Circuit Used For Bench Test

filtering. It cannot be placed on the DUT since its charge time would prohibit fast $V_{CC}$ switching at the DUT. This test circuit provided an approximate 40ns $V_{CC}$ rise time which was extremely fast relative to the substrate bias stabilization times of over 100us. The duty cycle of the input pulse is kept very low to prevent the device from self-heating.

3.4.9.2 Tektronix Test Circuit

The bench circuit of Figure 3.5 was expanded to provide a circuit that could be controlled automatically by the Tektronix system. The resulting circuit was revised twice to obtain a circuit compatible with the Tektronix hardware and software.

1st Automatic Test Approach - The intended operation of the circuit in Figure 3.6 and the associated Tektronix software is described by the following steps and the timing waveforms also in Figure 3.6.

Step 1 - The S-3270 applies the programmable signal F to the test circuit. As the signal propagates toward the base of Q1, it is delayed approximately 3ms by R1 and

C1. The delay allows the Tektronix to execute Step 2 and partially execute Step 3 before Q1 turns on to apply $V_{CC}$ to the DUT.

Step 2 - The Tektronix system executes a variable "wait" - initially set to 0us.

Step 3 - The R2942 algorithmic pattern generator tests the DUT for proper operation, using a March test pattern.

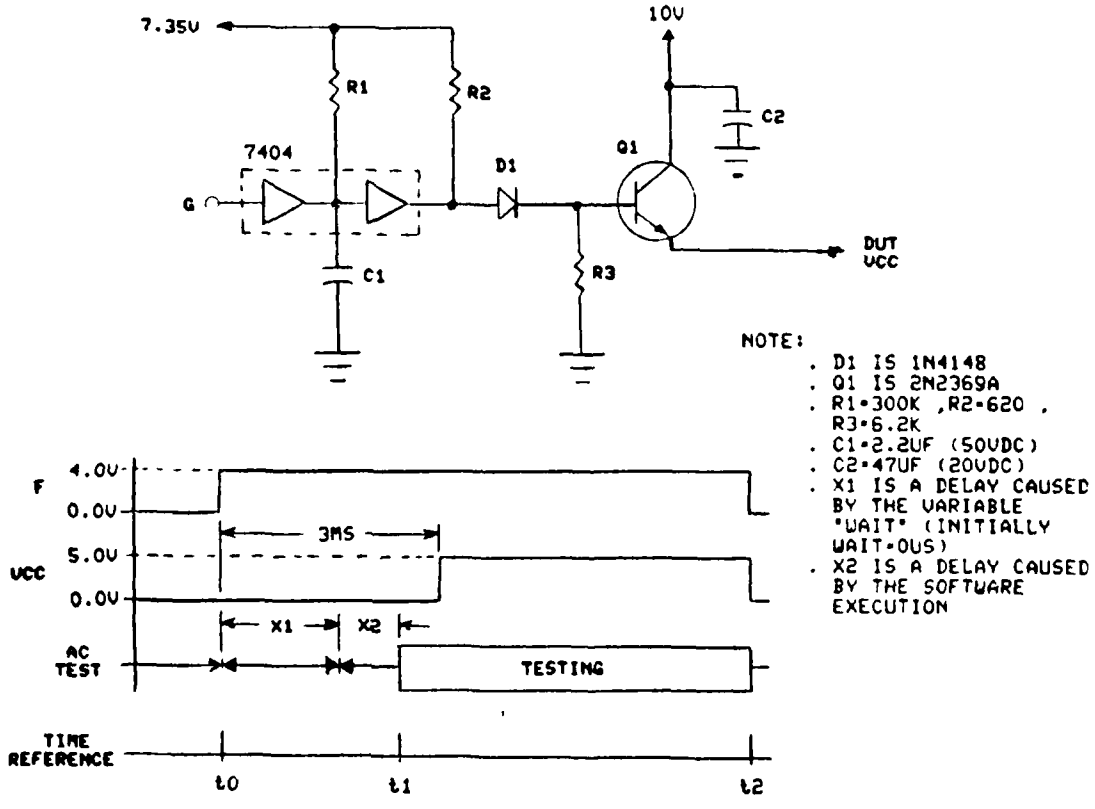



Figure 3.6 1st Test Circuit for Automatic Power-up Readiness Test

A test failure indicates that execution of the test pattern began before or too soon after $V_{CC}$ was applied. Each time the device fails, the wait in Step 2 is increased. Eventually a time relationship between $V_{CC}$ and the test pattern execution is reached that allows the DUT to pass testing. This would be the power-up time that is being sought. The duty cycle of the $V_{CC}$ switching is kept to approximately 5% to allow temperature and voltage transients to die out before $V_{CC}$ is reapplied.

This test approach assumed that the execution time indicated in Figure 3.6 could be established accurately and then be factored into subsequent time measurements. Unfortunately, the execution times were not consistent enough to permit accurate time measurement. Failure of this approach led to the 2nd test circuit.

2nd Automatic Test Approach - To overcome the difficulty encountered in the first approach, the circuit was modified to that in Figure 3.7. In this case, the $V_{CC}$ voltage at the DUT is directly related to the larger of the $F_1$ and $F_2$ signals. $F_1$ and $F_2$ are controlled by the 2942 test pattern. Therefore, any inconsistency in the 2942 starting time is irrelevant.

When the 2942 is started, it issues an $F_1$ signal that is gated by a programmable clock phase. The signal does not arrive at the $F_1$ input until the starttime delay of the clock phase has elapsed. Initially this delay is set to zero. After issuing $F_1$ the 2942 decrements an internal counter to provide a fixed delay which gives the DUT ample time to stabilize following the application of $V_{CC}$ via $F_1$. At the end of this fixed delay, the 2942 issues $F_2$ and simultaneously begins exercising the DUT. Since $F_2$ is not gated it appears instantly at the input and remains there throughout testing of the DUT. $F_1$ is gated by a phase whose maximum width is less than the test time. Therefore $F_1$ will fall back to zero before the end of the test, but $V_{CC}$ is sustained by the presence of $F_2$.

When the DUT passes the test with $F_1$ at the current starttime delay, the delay is increased which effectively pushes $V_{CC}$ turn on closer to the beginning of the DUT test. Repetitive $V_{CC}$-on-test-$V_{CC}$-off cycles with proper adjustment of the $F_1$ start delay for each cycle will eventually identify the minimum delay between power-up and proper device operation.

A difficulty with this technique is that when both signals $F_1$ and $F_2$ are high the Tektronix drivers are sharing the current load of the circuit. When one driver goes low, the remaining driver picks up the whole load. Since the drivers have high output impedance, the voltage drops, causing a corresponding step change in $V_{CC}$ as shown in Figure 3.7. Since the effect of the step on chip operation was

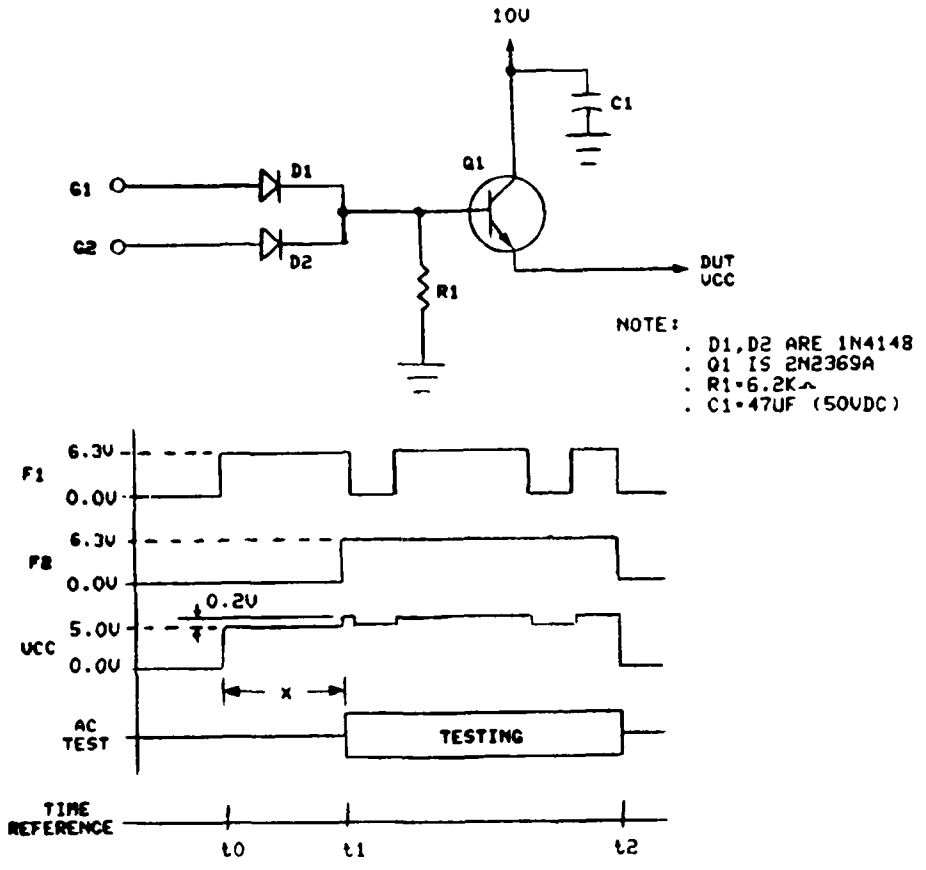



Figure 3.7 2nd Test Circuit for Automatic Power-up Readiness Test

unknown, the circuit was modified as described in the following paragraphs to eliminate the step.

3rd Automatic Test Approach - The circuit that was successfully used to measure power readiness is shown in Figure 3.8. A 7404 gate was placed in series with the inputs to isolate them from the changing current load of the circuit. The timing for this circuit is essentially the same as in the 2nd approach.

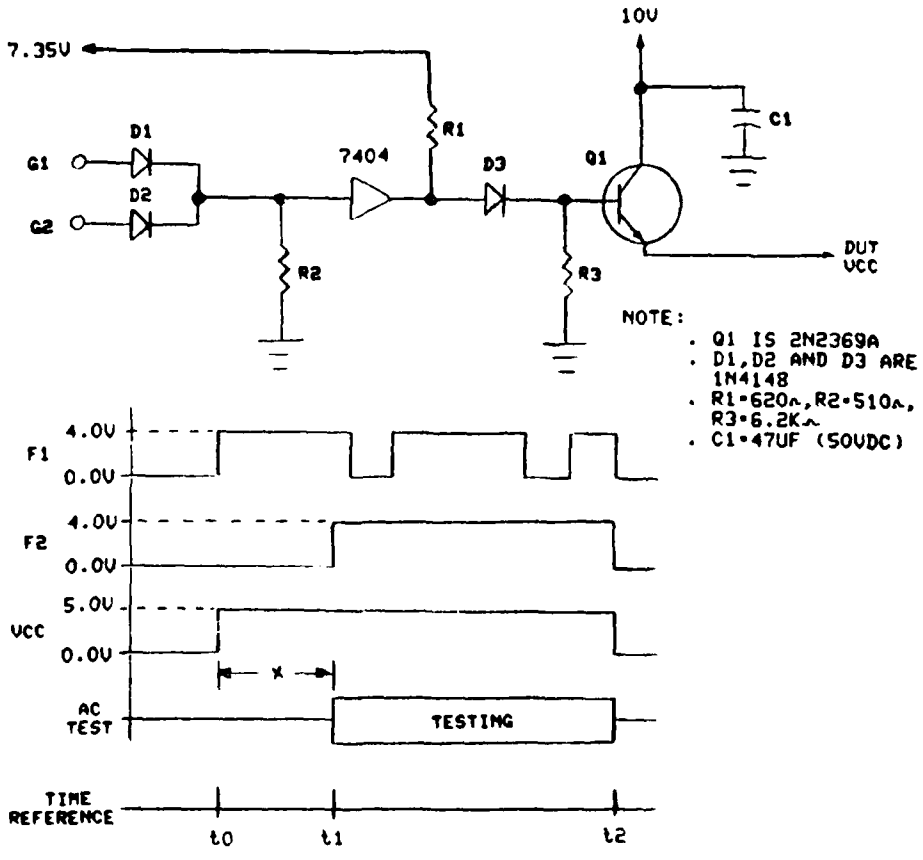



Figure 3.8 Final Test Circuit for Automatic Power-up Readiness Test

# 4. CHARACTERIZATION RESULTS

Table 1.1 on page 1 lists the number of devices received from each vendor. Not all of these parts went through the entire characterization process. Five parts from Vendor A were low speed versions, having different AC specifications, but identical DC specifications compared to the remaining Vendor A parts. Therefore, AC characterization data was not taken on the five devices. Devices that greatly exceeded the vendor specified limits during incoming testing or any time during subsequent AC and DC characterization were also removed from the process. Devices that passed commercial limits but failed at military temperatures or voltages were not rejected since all devices were rated as commercial.

Table 4.1 lists the number of devices from each vendor that were characterized. One Vendor D part ceased to function some time after the AC characterization and began to draw excessive supply current. This part was rejected from the full DC characterization.

Table 4.1 Number Of Devices Characterized

| Vendor | DC Char. | AC Char. |
|---|---|---|
| A | 24 | 18 |
| B | 16 | 16 |
| C | 3 | 4 |
| D | 2 | 2 |

## 4.1 DC Parameters

Table 4.2 lists the DC parameters and test conditions specified by each of the four vendors. For the DC characterization, the vendor specified conditions were applied, except during the supply current measurements on Vendor A and B parts. These two vendors specify a 5.25V maximum supply voltage limit. The characterization software applied 5.5V to all devices during the supply current measurements.

### 4.1.1 Leakage Current

Vendors A, B, and D specify a 10uA limit for the input leakage and the output high impedance leakage. Vendor C uses a 10uA limit for inputs but has a 50uA output limit. Vendor C's device has much greater output drive capability than the other types. The output gates therefore, probably use a larger surface area. The larger area could experience greater leakage, requiring a higher specified limit.

Leakage measurements were performed at -55°, 0°, 25°, 70°, and 125°C. Only one device (one from Vendor B) exceeded the limits. In general, all measurements yielded extremely low currents of 100nA or less. Currents of this amplitude are typical in LSI devices using MOS technology.

| PARAMETER | VENDOR A MIN | VENDOR A MAX | VENDOR B MIN | VENDOR B MAX | VENDOR C MIN | VENDOR C MAX | VENDOR D MIN | VENDOR D MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| POWER SUPPLY VOLTAGE | 4.75 | 5.25 | 4.75 | 5.25 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| POWER SUPPLY CURRENT | - | 125 | - | 90 | - | 120 (Standby - 20) | - | 145 | mA |
| INPUT LEAKAGE CURRENT | -10 | 10 | - | 10 | -10 | 10 | -10 | 10 | uA |
| OUTPUT LEAKAGE CURRENT (OUTPUTS DE-SELECTED) | -10 | 10 | - | 10 | -50 | 50 | -10 | 10 | uA |
| LOW-LEVEL INPUT VOLTAGE | -0.3 | 0.8 | -1.0 | 0.8 | -2.5 | 0.8 | -0.5 | 0.8 | V |
| HIGH-LEVEL INPUT VOLTAGE | 2.2 | $V_{CC}$+.5V | 2.0 | 5.25 | 2.0 | 6.0 | 2.0 | 6.0 | V |
| STATIC OUTPUT VOLTAGE LOW-LEVEL | - | 0.4 $I_{OL}$ = 4mA | - | 0.4 $I_{OL}$ = 2mA | - | 0.4 $I_{OL}$ = 16mA | - | 0.4 $I_{OL}$ = 2.1mA | V |
| STATIC OUTPUT VOLTAGE HIGH-LEVEL | 2.4 | - $I_{OH}$ = -10.mA | 2.4 | - $I_{OH}$ = -200uA | 2.4 | - $I_{OH}$ = 4mA | 2.4 | - $I_{OH}$ -1.0mA | V |

Table 4.2 Vendor Specified DC Parameters

### 4.1.2 Logic Output Voltage ($V_{OH}$, $V_{OL}$)

All devices passed their specified $V_{OH}$ limit at all temperatures including the military extremes. To summarize the $V_{OH}$ results, the lowest value (one of eight for 2KX8, one of one for 16KX1 parts) from each device is used to calculate an average low value for each type. The average values versus temperature are plotted in Figure 4.1. Also shown are the vendor specified output current conditions ($I_{OH}$) used when performing the measurements.

Although Vendor B devices have good margins between the actual and the specified limit values, $I_{OH}$ is very small relative to all other vendors. This indicates a relatively high resistance somewhere in the output stage. The large difference from the other types in output capability is a significant factor in assessing interchangeability.

As with $V_{OH}$, all devices passed the vendor specified $V_{OL}$ limits at all temperatures. To summarize the $V_{OL}$ results, the largest value from each device is used to calculate an average that is plotted for each vendor in Figure 4.2

For both $V_{OH}$ and $V_{OL}$, the two devices from Vendor D exhibited the worst case output voltages. Since they also exceeded the vendor's own $I_{CC}$ limit at 0°C and since only two devices were tested, the data may not be "typical".

### 4.1.3 Supply Current ($I_{CC}$)

Three supply current measurements were performed on each device at each temperature:

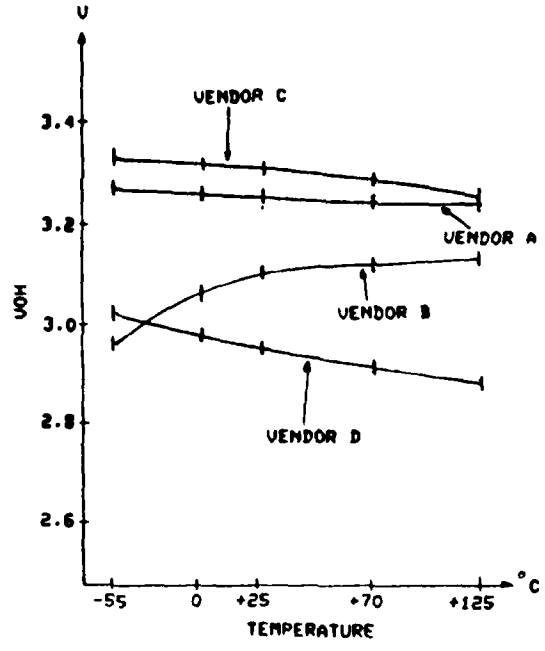
a) $I_{CC1}$ - measured during continuous read cycles.

b) $I_{CC2}$ - measured during continuous write cycles.

c) $I_{CC3}$ - measured while the chip is deselected (standby).

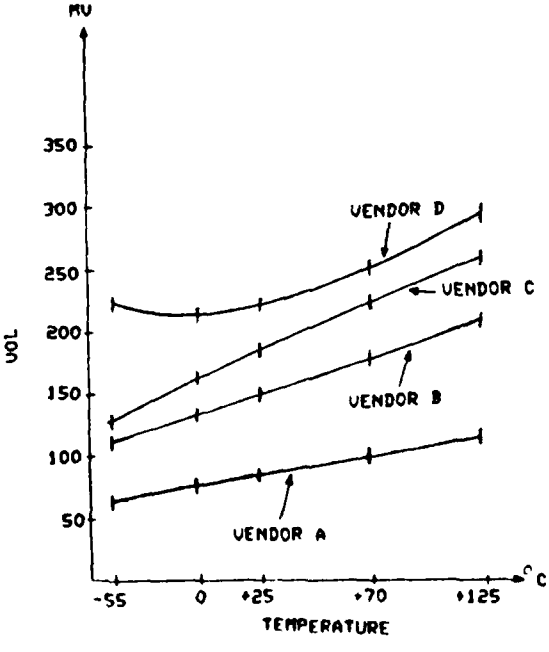
The average current of all devices from each vendor are plotted in Figure 4.3. Since the device from Vendor C has a chip deselect power down mode, its $I_{CC3}$ (standby) current is significantly less than its active current. Vendor D's part exhibits the highest current which varies little with the mode of operation. Since this part has the largest chip and cell area of the four types, and is fully static, it is not unusual that it has the highest supply current.

At 0°C, both parts from Vendor D slightly exceeded the 145mA 0°




| Vendor | $I_{OH}$ |
|---|---|
| A | -1.0 mA |
| B | -200 uA |
| C | -4.0 mA |
| D | -1.0 mA |

Figure 4.1 Average Of Minimum $V_{OH}$ Values




| Vendor | $I_{OL}$ |
|---|---|
| A | 4.0 mA |
| B | 2.0 mA |
| C | 16.0 mA |
| D | 2.1 mA |

Figure 4.2 Average Of Maximum $V_{OL}$ Values

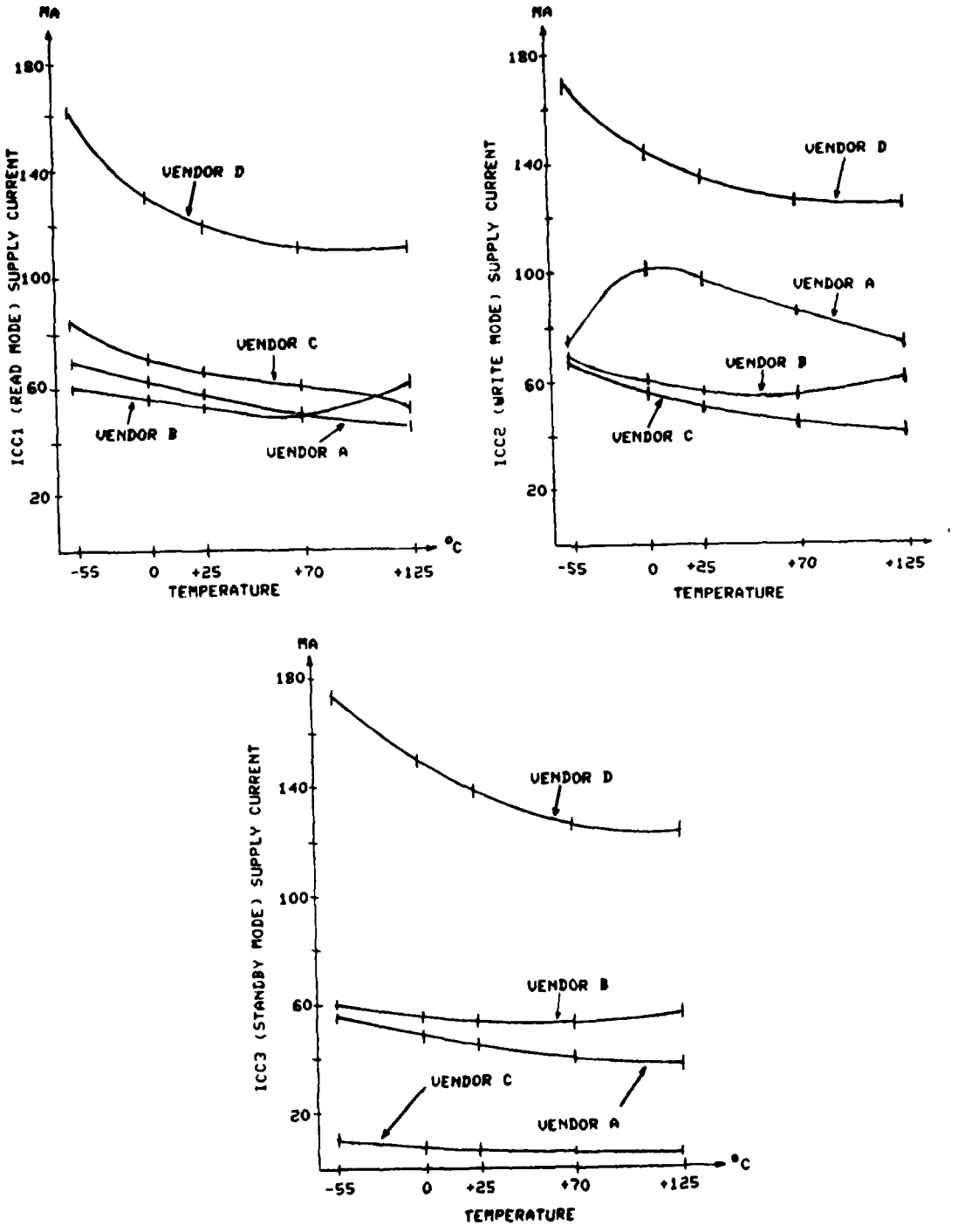



Figure 4.3 Average $I_{CC}$ During Read, Write and Deselect (Standby) Modes

to 70°C limit, but the sample size is too small to conclude that the limit is inadequately specified.

During $I_{CC}$ measurements, several devices from Vendor B exhibited erratic supply currents. Subsequent investigations found that at temperatures at or below 25°C, the substrate voltage would oscillate at a 5 to 5000Hz rate between zero and approximately 4 volts. Each time the voltage approached zero, the supply current dramatically increased. Presumably, the loss of substrate bias decreased transistor thresholds causing previously cut off transistors to conduct, increasing supply current. At these temperatures the devices suffered intermittent or continuous functional failures. As temperature was increased the substrate bias oscillations decreased, resulting in an average negative voltage, reduced supply current and improved performance.

These devices were eliminated from the characterization process.

## 4.2 Other Characteristics

### 4.2.1 Input/Output Pin Capacitance

Capacitance measurements were performed on selected pins of two or three parts from each vendor. Tables 4.3a through d list the measurement data and the vendor specified limits. (Note that the Vendor A "limits" are typical values.) Data on devices from Vendors B, C and D indicate good margins between actual values and the specified limits. For Vendor A, as might be expected, the data tends to "cluster" around the typical limits, giving a vague indication that the parts are acceptable. When military devices become available from Vendor A, a true maximum limit must be established to provide a definite accept/reject reference and to allow more accurate assessment of interchangeability.

### 4.2.2 Output Compare Thresholds

Many vendors, including Vendors A, C and D use 1.5V output compare levels when specifying AC parameters (Vendor B uses 0.6V and 2.2V references). Since output risetimes are not usually specified, the use of a 1.5V reference does not tell the user when to expect a valid logic level.

The AC parameter characterization used compare levels of 2.4V and 0.4V to correspond to the minimum $V_{OH}$ and maximum $V_{OL}$ levels specified by all four vendors. To provide some correlation between the output compare voltage reference and AC output parameters, worst case access times were determined using several different sets of output compare levels.

Figure 4.4 summarizes the data accumulated on the four device types. The plots for Vendors A, B and D represent averages of 7, 5 and 2 devices respectively. Only one Vendor C device was available for this segment of the 16K RAM evaluation. When the $V_{IL}$ compare voltage was being varied, the $V_{OH}$ compare voltage was set to 1.5V and vice versa.

At $V_{CC}$ = 4.5V all access time measurements exhibit considerable sensitivity to the output compare levels. Vendor B parts, for example, exhibit an average access time of 120ns when both output compare levels ($V_{LO}$ and $V_{HI}$) are equal to 1.5V. When $V_{HI}$ is set to 2.4V and $V_{LO}$ to 0.4V, the average access time measured is approximately 133ns. In general, for all device types at $V_{CC}$ = 4.5V, when 2.4V and 0.4V compare voltages are used, measured worst case access times are approximately 10% to 15% longer than when a single 1.5V compare level is used. A device driven by the memory would normally have maximum $V_{IH}$ and $V_{IL}$ input thresholds. A 1.5V referenced output parameter is not readily correlated to these input thresholds. On the other hand, 2.4V and 0.4V referenced parameters provide worst case information that is more easily related to the $V_{IH}$ and $V_{IL}$ limits. The input threshold limits are usually equal to or within the 2.4V and 0.4V output voltages, providing voltage margins and also timing margins.

Table 4.3a Vendor A Pin Capacitance

| VENDOR: A | | | | | |
|---|---|---|---|---|---|
| | CAPACITANCE | | | LIMIT | |
| PIN NO. | S/N = 100 | S/N = 101 | S/N = 120 | (TYP) | UNIT |
| 1 | 4.1 | 5.1 | 4.1 | 4 | pF |
| 2 | 3.6 | 4.2 | 3.7 | 4 | |
| 3 | 3.6 | 4.1 | 3.3 | 4 | |
| 4 | 3.5 | 4.0 | 3.1 | 4 | |
| 5 | 3.1 | 3.6 | 2.8 | 4 | |
| 6 | 3.1 | 3.7 | 2.9 | 4 | |
| 7 | 4.7 | 4.9 | 4.2 | 4 | |
| 8 | 4.7 | 4.9 | 4.1 | 4 | |
| 13 | 7.8 | 10.5 | 10.5 | 10 | |
| 14 | 8.5 | 11.5 | 11.0 | 10 | |
| 15 | 8.5 | 11.5 | 10.3 | 10 | |
| 18 | 4.9 | 5.4 | 4.7 | 4 | |
| 21 | 5.4 | 4.7 | 3.8 | 4 | |

Table 4.3b Vendor B Pin Capacitance

| VENDOR: B | | | | | |
|---|---|---|---|---|---|
| | CAPACITANCE | | | LIMIT | |
| PIN NO. | S/N = 20 | S/N = 6 | S/N = 13 | (MAX) | UNIT |
| 1 | 3.5 | 3.6 | 3.7 | 8 | pF |
| 2 | 3.2 | 3.3 | 3.4 | 8 | |
| 3 | 3.0 | 3.1 | 3.2 | 8 | |
| 4 | 2.7 | 2.9 | 3.0 | 8 | |
| 5 | 3.9 | 4.3 | 4.7 | 8 | |
| 13 | 5.2 | 5.5 | 5.7 | 12 | |
| 14 | 5.0 | 5.2 | 5.5 | 12 | |
| 15 | 4.7 | 5.0 | 5.2 | 12 | |
| 16 | 4.4 | 4.7 | 4.9 | 12 | |
| 17 | 3.7 | 3.9 | 4.1 | 12 | |
| 19 | 3.0 | 3.2 | 3.2 | 8 | |
| 20 | 3.7 | 4.2 | 4.5 | 8 | |
| 21 | 4.0 | 4.5 | 4.9 | 8 | |

Table 4.3c Vendor C Pin Capacitance

| VENDOR: C | | | | |
|---|---|---|---|---|
| PIN NO. | CAPACITANCE | | LIMIT (MAX) | UNIT |
| | S/N = 251 | S/N = 252 | | |
| 1 | 2.0 | 1.7 | 3 | pF |
| 2 | 1.8 | 1.7 | 3 | |
| 3 | 1.7 | 1.6 | 3 | |
| 4 | 1.6 | 1.6 | 3 | |
| 8 | 3.8 | 4.0 | 7 | |
| 9 | 2.1 | 2.5 | 3 | |
| 11 | 2.2 | 2.2 | 6 | |
| 12 | 2.1 | 2.1 | 3 | |
| 13 | 2.0 | 2.0 | 3 | |
| 14 | 2.0 | 1.8 | 3 | |
| 17 | 1.8 | 1.8 | 3 | |
| 18 | 1.9 | 2.2 | 3 | |
| 19 | 2.4 | 2.5 | 3 | |

Table 4.3d Vendor D Pin Capacitance

| VENDOR: D | | | | |
|---|---|---|---|---|
| PIN NO. | CAPACITANCE | | LIMIT (MAX) | UNIT |
| | S/N = 201 | S/N = 202 | | |
| 1 | 3.0 | 2.9 | 6 | pF |
| 2 | 3.0 | 2.8 | 6 | |
| 3 | 2.8 | 2.8 | 6 | |
| 4 | 3.0 | 3.0 | 6 | |
| 5 | 3.5 | 3.2 | 6 | |
| 13 | 3.5 | 3.2 | 6 | |
| 14 | 3.5 | 3.5 | 6 | |
| 15 | 3.4 | 3.5 | 6 | |
| 16 | 3.5 | 3.7 | 6 | |
| 17 | 3.5 | 3.7 | 6 | |
| 19 | 3.5 | 3.7 | 6 | |
| 20 | 3.5 | 3.8 | 6 | |
| 21 | 4.0 | 4.2 | 6 | |

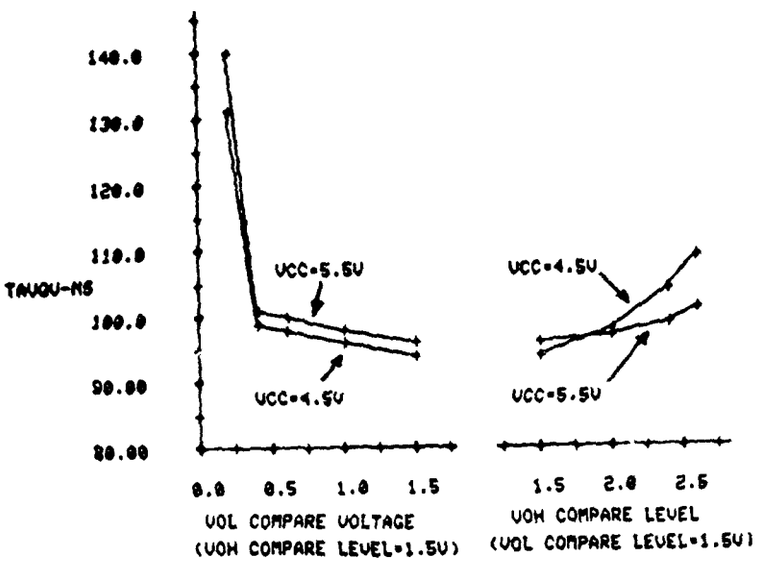



Figure 4.4a Vendor A - Output Compare Threshold Sensitivity
(average of 7 devices)

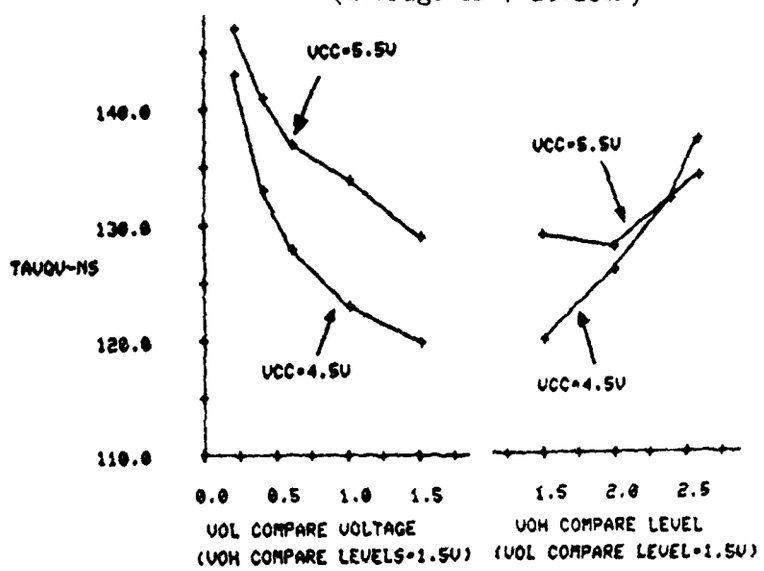



Figure 4.4b Vendor B - Output Compare Threshold Sensitivity
(average of 5 devices)

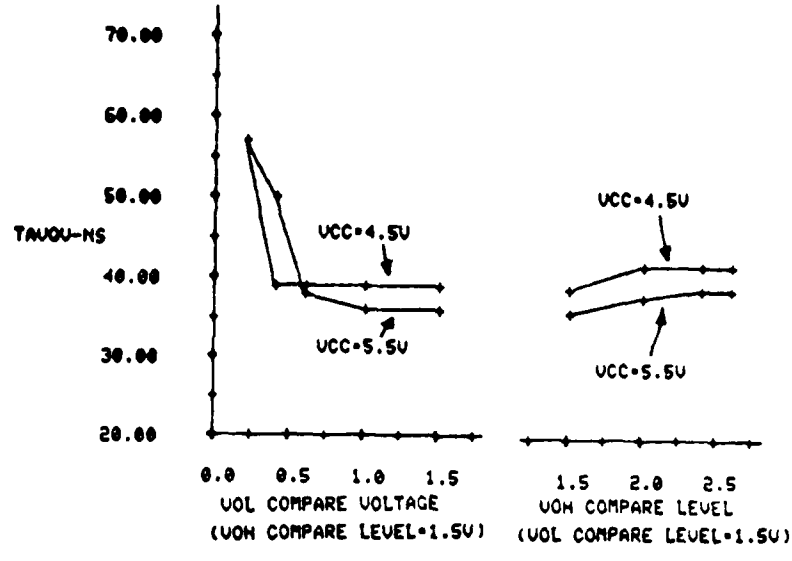



Figure 4.4c Vendor C - Output Compare Threshold Sensitivity
(1 device)

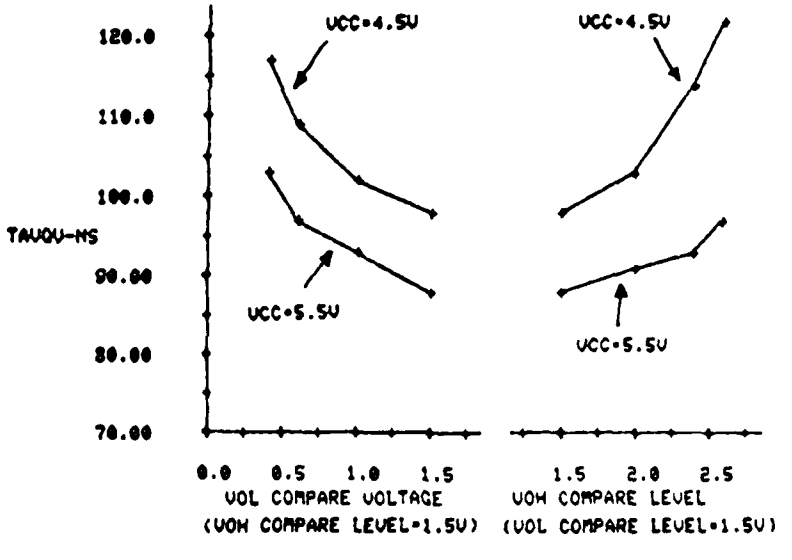



Figure 4.4d Vendor D - Output Compare Threshold Sensitivity
(average of 2 devices)

### 4.2.3 Output Disable Time

As described in section 3.4.3, two methods were used to designate when an output reached the high impedance state: 1) when output current decreased to zero, and 2) when the output voltage changed 0.5V from its initial stable logic voltage. The second method is frequently used and is easily implemented on an automatic tester, but is not necessarily accurate due to RC characteristics of the external load circuit. The first method is more accurate but difficult to implement on an automatic tester. Therefore, the first method is used to determine the actual disable time of an output on several devices and to determine effectiveness of the second method.

Tables 4.4a and 4.4b list the data that was accumulated on devices from Vendors A, B and C. Due to their late arrival and the restrictive time schedule, Vendor C devices were not subjected to these tests.

The data indicates that external capacitance has little effect on the actual disable time of all three device types. On the other hand, capacitance significantly affects measurements that use the output voltage as a reference. Values obtained with this method are extremely misleading, causing devices to appear much slower than they really are. Until an accurate automatic test method is developed, it is recommended that any voltage reference method be avoided unless it is performed on the bench with very low load capacitance (parasitic or external component).

Although Vendors A and B use output voltage references for the disable time limits, the data in Tables 4.4a and b cannot be correlated to the limits. Both vendors specify load circuit that use 100pF capacitance and that do not guarantee that output voltage will reach the specified high impedance reference level.

Vendor D indicates that turn off time is referenced to the actual high impedance condition. The data taken using the first method of reference is well within the 60ns limit used by Vendor D.

### 4.2.4 Input Threshold Voltage

The input threshold voltages of each input were measured at three temperatures on four Vendor A and four Vendor B parts and one part from Vendor D. The highest logic high threshold and lowest logic low threshold from each device is listed in Table 4.5.

Table 4.4a Output Disable Time - Output Initially At Logic One

Vendor: A Limit = 35ns

| S/N | 110 | | | 112 | | | 123 | | | 124 | | | 130 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Load | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | pF |
| A | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | ns |
| B | 62 | 104 | 148 | 62 | 109 | 138 | 66 | 105 | 148 | 58 | 92 | 132 | 66 | 96 | 128 | ns |

Vendor: B Limit = 120ns

| S/N | 6 | | | 9 | | | 21 | | | 24 | | | 29 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Load | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | pF |
| A | 30 | 30 | 30 | 38 | 28 | 28 | 22 | 20 | 20 | 20 | 24 | 24 | 24 | 24 | 24 | ns |
| B | 83 | 138 | 178 | 80 | 130 | 178 | 78 | 118 | 148 | 68 | 133 | 152 | 68 | 130 | 158 | ns |

Vendor: D Limit = 60ns

| S/N | 201 | | | 202 | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Load | 15 | 35 | 50 | 15 | 35 | 50 | | | | | | | | | | pF |
| A | 8 | 8 | 8 | 8 | 8 | 8 | | | | | | | | | | ns |
| B | 76 | 109 | 154 | 66 | 104 | 132 | | | | | | | | | | ns |

A = point at which output current reaches zero.

B = point at which output voltage decreases by 0.5V.

Table 4.4b Output Disable Time - Output Initially At Logic Zero

Vendor: A Limit = 35ns

| S/N | 110 | | | 112 | | | 123 | | | 124 | | | 130 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Load | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | pF |
| C | 18 | 18 | 18 | 18 | 18 | 18 | 19 | 19 | 19 | 17 | 16 | 16 | 16 | 15 | 15 | ns |
| D | 23 | 28 | 33 | 23 | 31 | 33 | 24 | 31 | 34 | 22 | 29 | 34 | 20 | 28 | 33 | ns |

Vendor: B Limit = 120ns

| S/N | 6 | | | 9 | | | 21 | | | 24 | | | 29 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Load | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | 15 | 35 | 50 | pF |
| C | 19 | 19 | 19 | 21.5 | 23 | 23 | 15 | 17 | 17 | 19 | 19 | 20 | 17 | 19 | 19 | ns |
| D | 58 | 64 | 68 | 56 | 62 | 67 | 45 | 54 | 55 | 49 | 57 | 64 | 51 | 58 | 64 | ns |

Vendor: D Limit = 60ns

| S/N | 201 | | | 202 | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Load | 15 | 35 | 50 | 15 | 35 | 50 | | | | | | | | | | pF |
| C | 10.5 | 11 | 12 | 12 | 12 | 12 | | | | | | | | | | ns |
| D | 20 | 33 | 34 | 17 | 28 | 36 | | | | | | | | | | ns |

C = point at which output current reaches zero.
D = point at which output voltage increases by 0.5V.

Table 4.5 Worst Case Input Threshold Voltages

| | Input High Threshold | | | Input Low Threshold | | |
|---|---|---|---|---|---|---|
| | -55° | 25° | 125° | -55° | 25° | 125° |
| Vendor A (SN) | | | | | | |
| # 121 | 1.6 | 1.5 | 1.5 | 1.3 | 1.3 | 1.2 |
| # 125 | 1.7 | 1.6 | 1.6 | 1.2 | 1.3 | 1.2 |
| # 127 | 1.6 | 1.6 | 1.5 | 1.3 | 1.3 | 1.2 |
| # 117 | 1.8 | 1.8 | 1.7 | 1.3 | 1.3 | 1.2 |
| Vendor B (SN) | | | | | | |
| # 13 | 1.7 | 1.6 | 1.5 | 1.5 | 1.4 | 1.4 |
| # 25 | 1.7 | 1.5 | 1.4 | 1.5 | 1.3 | 1.3 |
| # 27 | 1.6 | 1.5 | 1.4 | 1.4 | 1.3 | 1.3 |
| # 24 | 1.6 | 1.5 | 1.4 | 1.4 | 1.3 | 1.3 |
| # 23 | 1.7 | 1.5 | 1.4 | 1.4 | 1.3 | 1.3 |
| Vendor D (SN) | | | | | | |
| # 201 | 1.5 | 1.4 | 1.4 | 1.4 | 1.3 | 1.3 |

Comparing values between Vendors A and B, one can see that Vendor A's worst case input hign and low thresholds are less favorable than Vendor B's. When comparing noise margins, Vendor A has slightly more favorable margin for logic high voltages since they specify a 2.2V $V_{IH}$ limit, while Vendor B specifies 2.0V. This comparison of static threshold voltages is, however, misleading. As subsequent discussion will indicate, Vendor A devices exhibit significant sensitivity to logic input levels under dynamic conditions. They do not operate well with input high and low levels set to 2.2V and 0.8V. Vendor B parts on the other hand, show less sensitivity to logic levels and perform well with input voltages at 2.0V and 0.8V.

4.2.5 Input Logic Level Sensitivity

Figure 4.5 summarizes worst access times at various input voltage levels for the indicated number of devices. The measurements were performed at 25°C while using a March pattern. Each set of axes in the figure consists of two sets of lines. The left-hand set represents worst case access time versus input low voltage with input high voltage set at 3.0V. The right-hand set represents access time versus input high voltage with input low voltage at 0.4V.

The data from Vendors B, C and D show little sensitivity to logic levels that are equal to or more optimal than 2.0V and 0.8V. These voltages are the specified limits of Vendor B, C, and D. Of the three vendors, Vendor B exhibits the largest shift in access time. At $V_{CC}$ = 5.5V the average access time is approximately 150ns for $V_{IH}$ = 2.0V. At $V_{IH}$ = 3.0V for the same $V_{CC}$, the average worst case access time is slightly more than

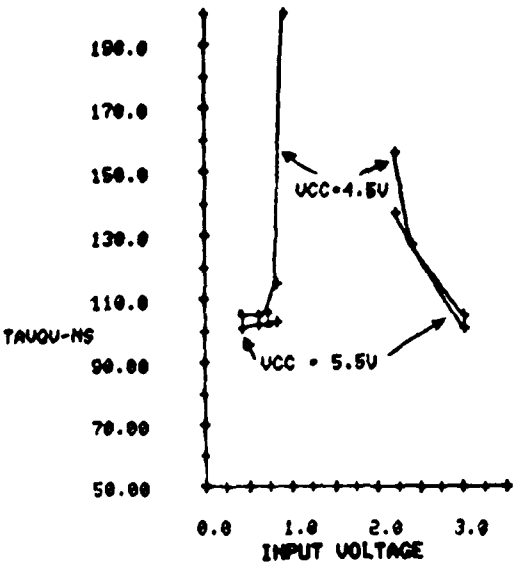



Figure 4.5a Vendor A - Input Logic Level Sensitivity

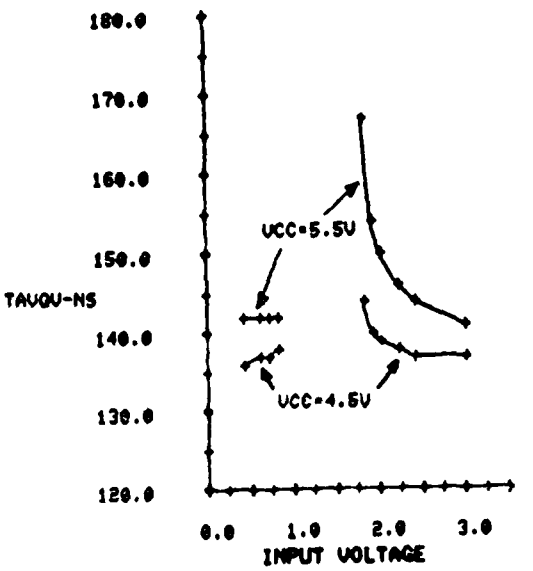



Figure 4.5b Vendor B - Input Logic Level Sensitivity

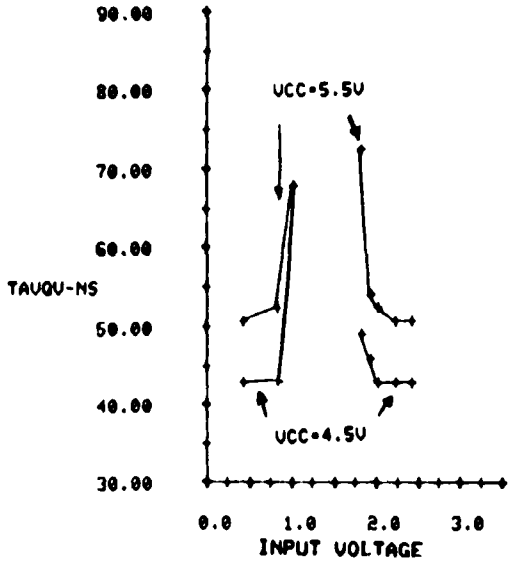



Figure 4.5c Vendor C - Input Logic Level Sensitivity

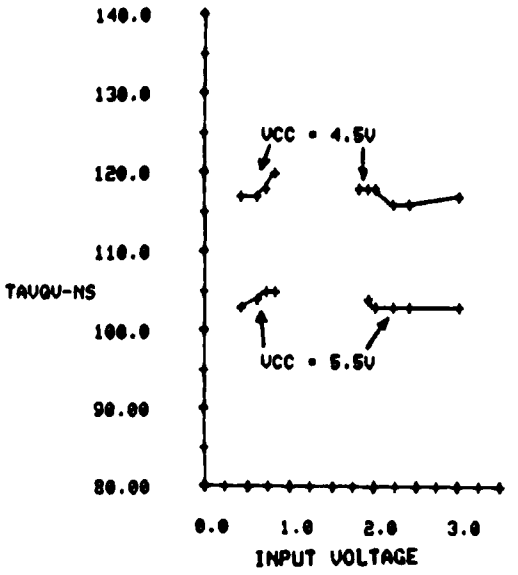



Figure 4.5d Vendor D - Input Logic Level Sensitivity

140 ns. On all parts, variations of the logic high levels have the greater impact on access time.

Vendor A parts exhibit somewhat greater sensitivity to logic low voltages than other vendors, but their response to logic high voltage is dramatic. At $V_{CC}$ = 4.5V and $V_{IH}$ at 2.0V the access times are greater than 300ns and are therefore not plotted. As the logic voltage approaches 2.4V, which is 0.2V within the vendor specified limit, the access times still do not come within the 120ns limit.

The logic level sensitivity of Vendor A devices is a serious disadvantage and discourages interchangeability with other vendor parts. When full military devices become available, a prime characterization goal should be to verify that improvements have been made in the dynamic input logic level operating range.

4.2.6 Pattern Sensitivity

Devices from Vendors A and B were subjected to 14 different test patterns during the pattern sensitivity study. At the time of the study, Vendors C and D were not considered potential military 16K RAM sources. Therefore, row and column related tests were not developed for these types since each would require a unique test adapter. Existing adapters were used to apply "black box" type test patterns to these part types. Herein "black box" type test patterns are those not designed for a particular row or column arrangement.

All test patterns used during the 16K RAM study are described in the Appendix. Table 4.6 is a summary of the access times measured on devices from each vendor using the various patterns. To minimize logic level effects, measurements were performed with input logic levels at 3.0V and 0.4V. The data from Vendors A and B represent averages of the indicated number of devices. Only one device from each of Vendors C and D was used in the study.

The March pattern compares well with the $n^2$ tests, Galloping and Inter Address, for all four device types. The Read/Write Address Complement also compares favorably.

Vendor A parts show slightly less sensitivity to row patterns than to column and black box patterns. This may be due to the relatively long columns whose charge times may significantly impact the worst case access times during patterns that exercise the columns.

Although Vendor A parts are somewhat more sensitive to some patterns than others, the worst case access time does not differ more than 6ns. This small difference is probably due to the internal address circuitry that causes decoder outputs to return to the same state prior to initiating a new row/column selection. Therefore, the previous address

| | March | Galloping | Galloping Row | Galloping Column | Inter-Address Write Recovery | Inter-Row Write Recovery | Inter-Column Write Recovery | Read/Write Address Complement | Read/Write Row Complement | Read/Write Column Complement | Write/Write Address Complement | Write/Write Row Complement | Write/Write Column Complement | Sliding Diagonal |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Vendor A (Aver. of 11 dev.) | 96 | 96 | 92 | 96 | 96 | 92 | 96 | 92 | 91 | 92 | 90 | 91 | 90 | 94 |
| Vendor B (Aver. of 10 dev.) | 142 | 144 | 129 | 138 | 146 | 131 | 140 | 143 | 139 | 134 | 143 | 143 | 136 | 119 |
| Vendor C (1 device) | 53 | 52 | - | - | 53 | - | - | 53 | - | - | 53 | - | - | - |
| Vendor D (1 device) | 112 | 108 | - | - | 112 | - | - | 112 | - | - | 108 | - | - | - |

NOTE: All times in nsec.

Table 4.6 Test Pattern vs. Worst Case Access Time

has little bearing on the decoder response to a new address.

When complement type patterns are used, Vendor B parts show more sensitivity to those related to rows. When Gallop and Inter-Address type patterns are used, the parts show more sensitivity to those related to columns. In general, neither column or row related patterns compare as well to $n^2$ patterns as do the black box types.

For Vendor B the sliding diagonal pattern is very poor for measuring worst case access times. It is suspected that the low access times are due to the infrequent data output transitions. Read operations are performed along diagonals of like data and only one diagonal has opposite data. A slow address decode rarely results in unexpected output data even if it originates from the wrong location. The Sliding Diagonal Test is designed to verify that each cell can store a data bit opposite to the other cells in the associated row and column.

The pattern sensitivity data supports the use of March and Address Complement patterns as effective replacements for Gallop and Inter-Address patterns for all four types. Although some row or column patterns are also as effective, they require a unique test adapter for each part type and knowledge of which address pins connect to row and column decoders. This knowledge is usually obtainable, but row/column related patterns are contrary to the idea of standardization. Since March and Address Complement are black box type patterns, they can be applied, without modification, to different device types that are pin compatible. Only one test adapter for each pin configuration is required. It is recommended that any MIL-M-38510 slash sheets developed for these parts specify the March or Address Complement type patterns for verifying access times.

4.2.7 Staggered Address Test

This test was intended to verify that a "late" address bit on Vendor A parts would initiate a new read cycle even if one was already in progress. This was performed by delaying one address bit from all others and measuring worst case access time from that bit. Ideally the access time relative to that bit should be constant regardless of its delay from the remaining bits. It was found that this situation did in fact occur.

Incrementally adjusting $A_0$ from 0ns delay to greater than 300ns found that the access time relative to $A_0$ did not change.

This technique verified the circuit operation during the read function, but had it been used during a write cycle, a circuit anomaly would have been detected. Through other users and through the vendor, it was learned that if one or more address bits are delayed from the remaining bits during an intended write cycle, a write operation would not perform correctly. For this reason, according to the vendor, the part is being redesigned.

### 4.2.8 Power-up Readiness

The power-up readiness tests consisted of two parts:

1) bench measurement of the time for the substrate voltage to stabilize after power is applied.

2) automatic measurement of the time delay between power-up and reliable device operation.

The measurements were obtained at -55°, 25° and 125°C. Vendor C parts were not available for the second set of measurements. This was not deemed critical since at that time they were not considered a potential military vendor.

Table 4.7 lists the bench data accumulated on the indicated parts at the three temperatures. Table 4.8 lists the automatic measurement data. A general comparison of the tables reveals that long before the substrate voltage has stabilized, the Vendor B and D devices are operating reliably. This suggests that only a slightly negative substrate bias voltage is necessary for device operation. Therefore, a relatively large margin exists between the required and the actual bias levels. Vendor A parts show considerably less margin.

Vendor A and Vendor B bias stabilization data indicates some sensitivity to temperature but in opposite directions. Vendor A stabilization times increase with temperature while Vendor B's decrease. Neither Vendor C or D devices show variation over temperature, but data on more devices must be taken before drawing a conclusion.

Vendor A is the only vendor that specifies a wait time after power-up before reliable operation is guaranteed. The data in Table 4.8 indicates in general that Vendor A's 2ms wait time is adequate even at 125°C.

Table 4.7 Substrate Voltage Stabilization Time

| VENDOR | S/N | Vsub. Stable Time -55°C | +25°C | +125°C |
|---|---|---|---|---|
| A | 114 | 600us | 600us | 650us |
| | 115 | 600us | 600us | 700us |
| | 119 | 600us | 600us | 700us |
| B | 13 | 280us | 200us | 190us |
| | 23 | 320us | 260us | 230us |
| | 24 | 600us | 280us | 200us |
| | 25 | 600us | 280us | 220us |
| | 27 | 750us | 360us | 240us |
| C | 251 | 50us | 50us | 50us |
| D | 202 | 100us | 100us | 100us |

Table 4.8 Power Up Readiness Time

| VENDOR | S/N | Power Up Time -55°C | +25°C | +125°C |
|---|---|---|---|---|
| A | 114 | 0us | 0us | 275us |
| | 115 | 0us | 142us | 318us |
| | 119 | 0us | 0us | 284us |
| | 129 | 0us | 0us | 10us |
| B | 13 | 0us | 10us | 11us |
| | 23 | 0us | 0us | 9us |
| | 24 | 0us | 0us | 0us |
| | 25 | 0us | 0us | 0us |
| | 27 | 0us | 0us | 19us |
| D | 201 | 0us | 0us | 3us |
| | 202 | 0us | 0us | 0us |

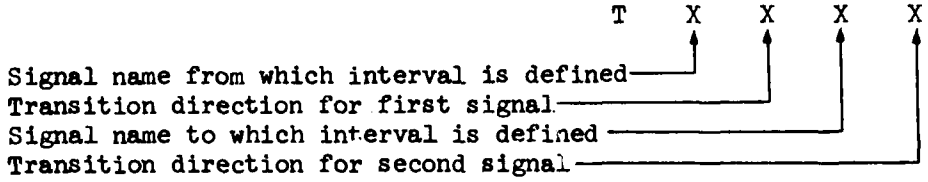
## 4.3 AC Characterization

Table 4.9 lists the AC parameters that were characterized and the vendor specified limits. The timing waveforms in Figures 4.6 and 4.7 illustrate the edge pairs associated with each parameter for the 2KX8 and the 16KX1 device configurations.

### 4.3.1 Timing Parameter Abbreviations and Waveform Symbols

The abbreviations and symbols discussed in this section are used in this report and have been standardized for slash sheet use.

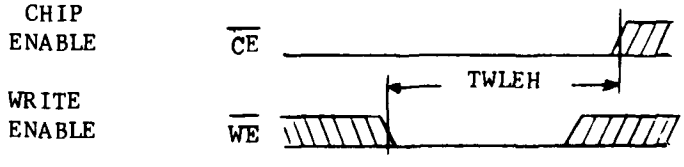
The initial timing abbreviation character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that defines a timing interval. The two descriptors for each signal point specify the signal name and the signal transition. Thus the format is:




a. Signal definitions:
   - A = Address
   - D = Data in
   - Q = Data out
   - W = Write enable
   - E = Chip enable

b. Transition definitions:
   - H = Transition to high
   - L = Transition to low
   - V = Transition to valid
   - X = Transition to invalid or don't care
   - Z = Transition to off (high impedance)

Example:




The example shows Write pulse setup time defined as TWLEH-Time from Write Enable low to Chip Enable high.

Table 4.9 Vendor Limits For AC Parameters

| | Vendor A | | Vendor B | | Vendor C | | Vendor D | |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max |
| TAVQV | - | 120n | - | 450n | - | 50n | - | 200n |
| TELQV | - | 60n | - | 450n | - | 55n | - | 70n |
| TOLQV | - | 60n | - | 450n | - | - | - | 70n |
| TWLWH | 45n | - | 400n | - | 25n | - | 120n | - |
| TAVWL | 0n | - | 0n | - | 45n | - | 0n | - |
| TDVWH | 10n | - | 400n | - | 20n | - | 120n | - |
| TELWH | 45n | - | 400n | - | 50n | - | 120n | - |
| TWHAX | 40n | - | 0n | - | 0n | - | 20n | - |
| TWHDX | 10n | - | 0n | - | 0n | - | 0n | - |
| TAXQX | 10n | - | 10n | - | - | - | 20n | - |

Output Compare Levels:

| | |
|---|---|
| Vendor A | 1.5V |
| Vendor B | 2.2V and 0.6V |
| Vendor C | 1.5V |
| Vendor D | 1.5V |

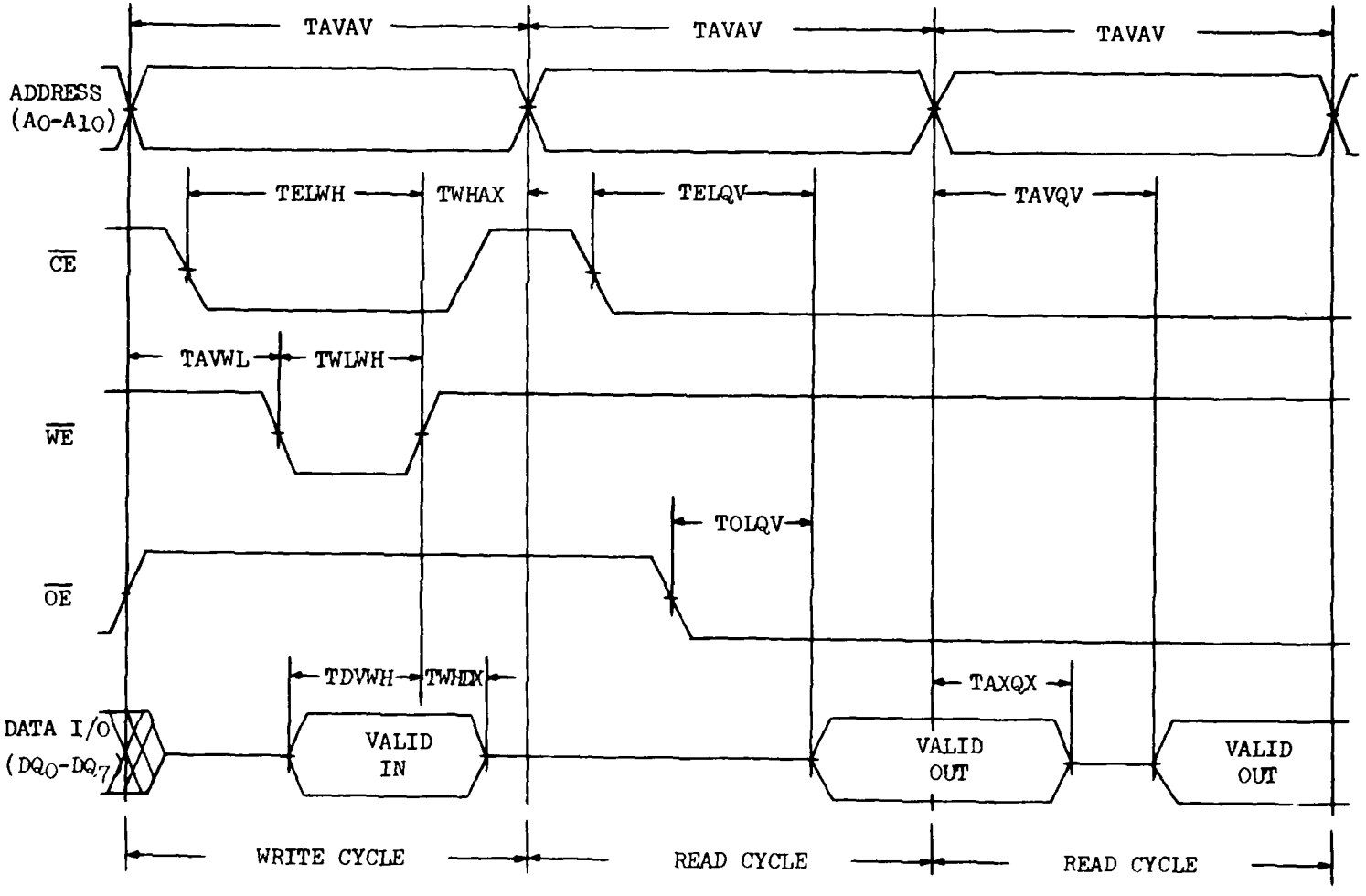



Figure 4.6 Timing Waveforms For 2KX8 Static RAM

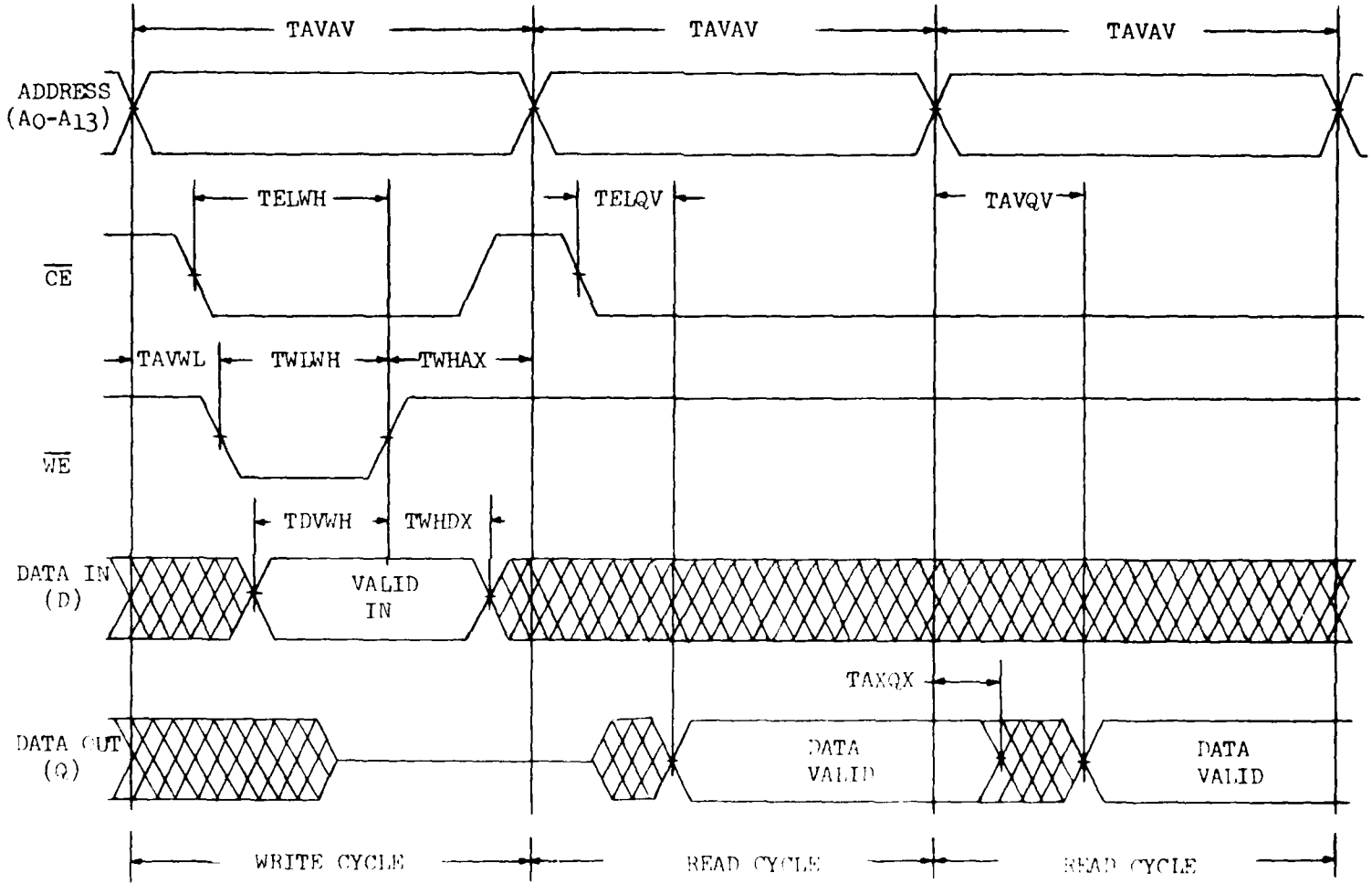
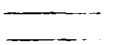
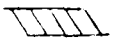
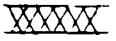
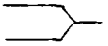



Figure 4.7 Timing Waveforms For 16K1 Static RAM

The waveform symbol definitions are as follows:

| WAVEFORM SYMBOL | INPUT | OUTPUT |
|---|---|---|
|  | MUST BE VALID | WILL BE VALID |
|  | CHANGE FROM H TO L | WILL CHANGE FROM H TO L |
|  | CHANGE FROM L TO H | WILL CHANGE FROM L TO H |
|  | DON'T CARE: ANY CHANGE PERMITTED | CHANGING: STATE UNKNOWN |
|  | OFF | HIGH IMPEDANCE |

All AC measurements discussed in this section were made with output compare levels of 2.4V and 0.4V.

4.3.2 Vendor A

Initial AC characterization results, using Vendor A specified input voltage limits were misleading. The sensitivity to the $V_{IH}$ limit of 2.2V was manifested as numerous functional and parametric failures. After investigation revealed the senstivity, AC parameters were measured using $V_{IH}$ and $V_{IL}$ levels of 3.0V and 0.4V. The results, in general, demonstrated good performance relative to the vendors AC limits.

4.3.2.1 Address, Chip Enable and Output Enable Access Times

Figures 4.8, 4.9 and 4.10 summarize the measurement results of address access time (TAVQV), chip enable access time (TEVQV), and output enable access time (TOVQV), at $V_{CC}$ = 4.5V and 5.5V. Each set of three points at one temperature represents minimum (min), average (avg), and maximum (max) parameter values. The values at each temperature are taken from the quantity of devices indicated by the number above the horizontal axis.

All three figures illustrate that within the commercial temperature range all 18 Vendor A devices meet their commercial specification even though $V_{CC}$ is beyond the 4.25V or the 5.25V vendor limits. Between 70° and 125°C, all three parameters show increases that demonstrate the same temperature response seen between lower temperatures. Note that at 125°C, TAVQV is beyond the 120ns limit. If this particular part type was qualified for a slash sheet, the TAVQV limit may have to be somewhat higher than 120ns.

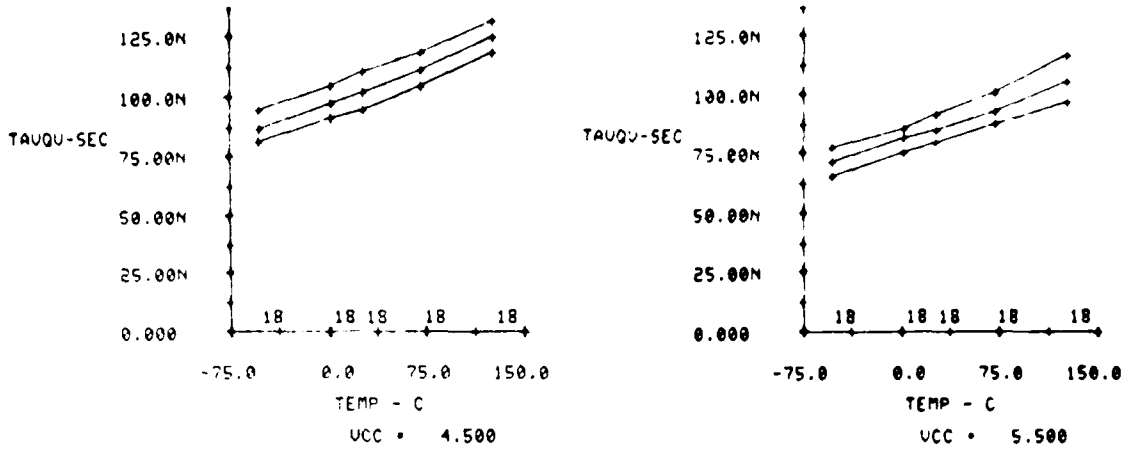



Figure 4.8 Vendor A - Min, Avg, Max Address Access Time Vs. Temperature

At -55°C and 5.5V two devices suffered functional failures. Although, not shown, at 5.25V, only one device failed. This sensitivity for high $V_{CC}$ at low temperature was also seen during the characterization of several other parameters. This sensitivity along with the input threshold problem will be considered when full military devices of the new design are characterized.

4.3.2.2 Address to Data Not Valid (TAXQX)

The plots in Figure 4.11 illustrate the minimum, average, and maximum times that the data remains valid after the current address is changed. Note that the minimum curve for both 4.5V and 5.5V drops below the 10ns limit. However, this is not due to device failure, but is due to the output voltage reference used. The characterization test used 2.4V and 0.4V for output references, while the vendor uses 1.5V. As the previously discussed output disable time data indicates, the discharge time of the output load affects output measurement data. Since the vendor uses a 1.5V reference it is expected that the time to discharge from 2.4V or the time to charge from 0.4V to 1.5V accounts for the difference in measured data from the specified limit.

4.3.2.3 Address Setup Time (TAVWL)

The TAVWL characteristics at $V_{CC}$ = 4.5V and 5.5V are shown in Figure 4.12. Several devices exhibited setup times greater than zero. The erratic response of several devices, causing the irregular line plots in

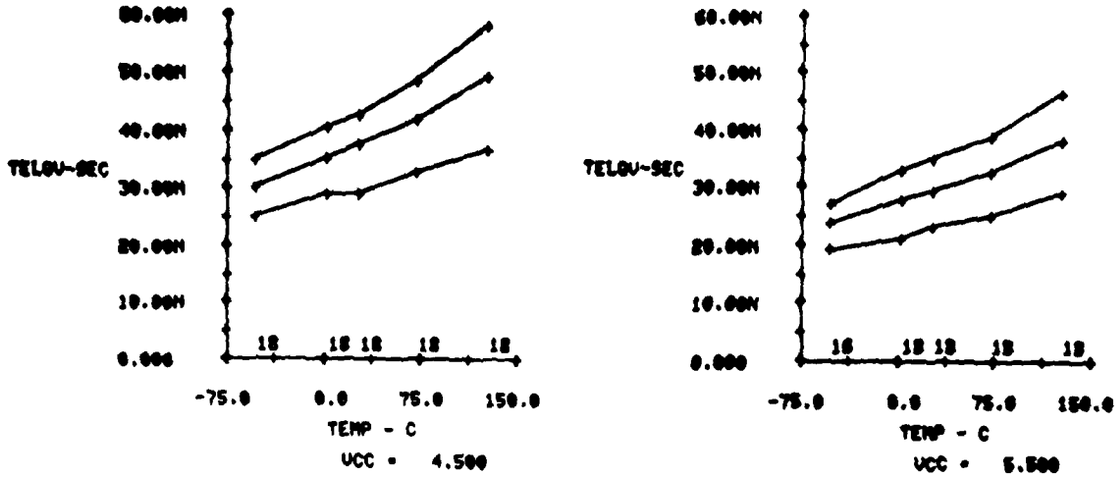



Figure 4.9 Vendor A - Min, Avg, Max Chip Enable Access Time Vs. Temperature

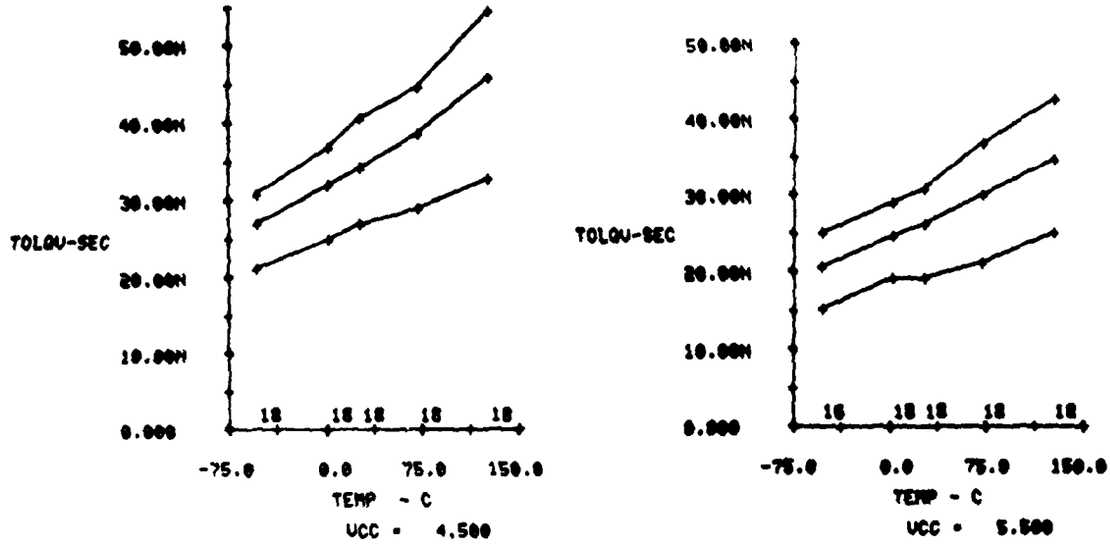



Figure 4.10 Vendor A - Min, Avg, Max Output Enable Access Time Vs. Temperature

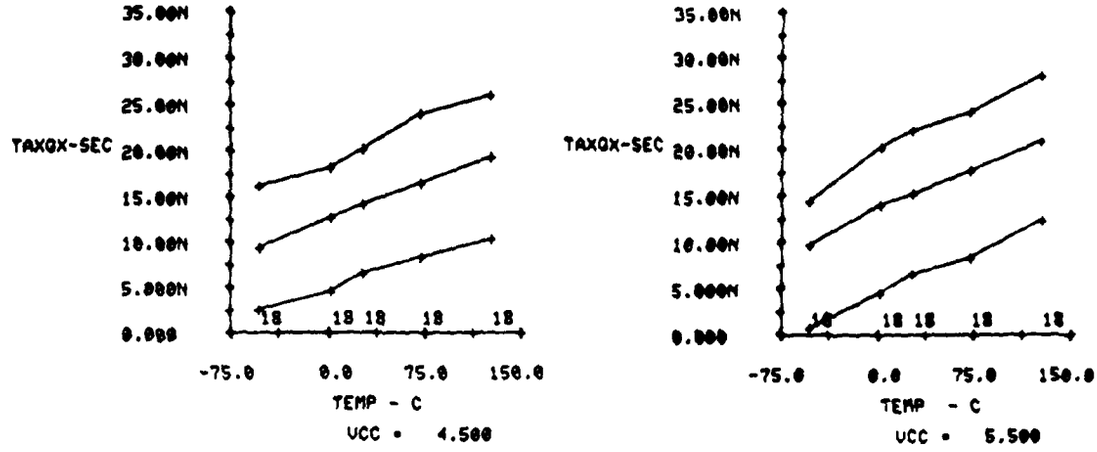



Figure 4.11 Vendor A - Min, Avg, Max Output Hold After Address Change Vs. Temperature

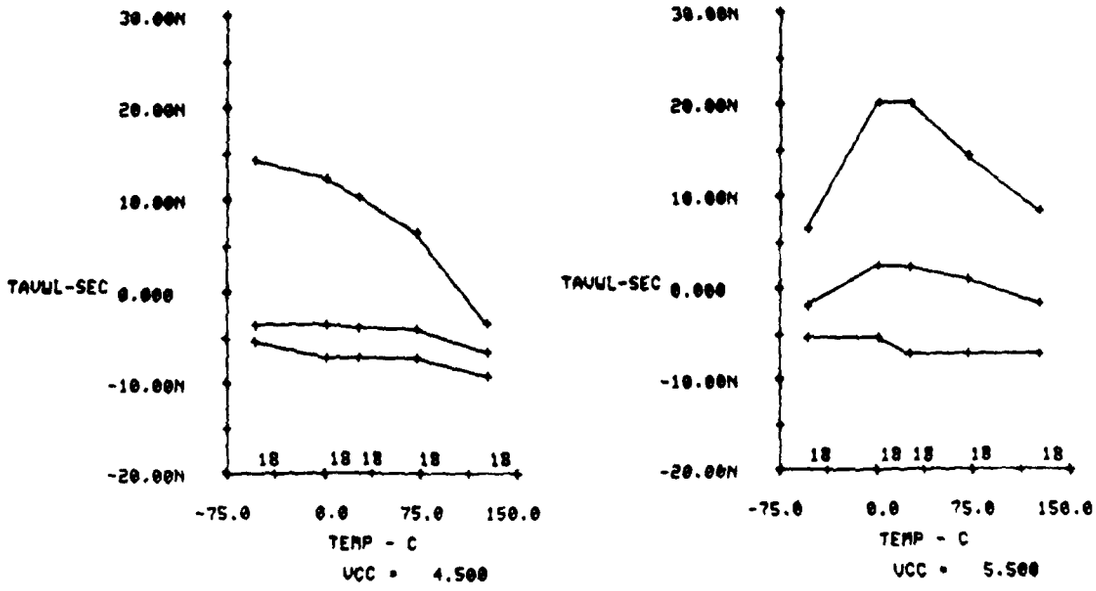



Figure 4.12 Vendor A - Min, Avg, Max Address Setup Time Vs. Temperature

Figure 4.12, may be due to the addressing anomaly which the vendor intends to eliminate through redesign. If this response appears during characterization of military devices, it should be investigated to relate it to other device characteristics in order to assess its full impact on performance.

4.3.2.4 Other AC Characteristics

The remaining AC parameters, TWLWH, TDVWH, TELWH, TWHAX, TWHDX were well within the vendor specified limits. Some functional failures occurred at -55°C when $V_{CC}$ was at 5.25V or 5.5V. These failures were attributed to a functional sensitivity to temperature and voltage mentioned earlier.

4.3.3 Vendor B

Relative to their own limits, the Vendor B parts performed extremely well. All parts that were characterized easily met the vendor limits within the commercial temperature range. One device failed at 125°C with $V_{CC}$ = 5.5V. Other devices had failures related to -55°C and lower $V_{CC}$ levels. Several of the devices rejected from the characterization also had the low temperature and low $V_{CC}$ sensitivity but to a greater degree. Vendor B is redesigning their device to extend the temperature operating range.

4.3.3.1 Address, Chip Enable and Output Enable Access Times

Figures 4.13, 4.14, and 4.15 summarize the results of the three types of access time measurements. Even at maximum temperature, all devices

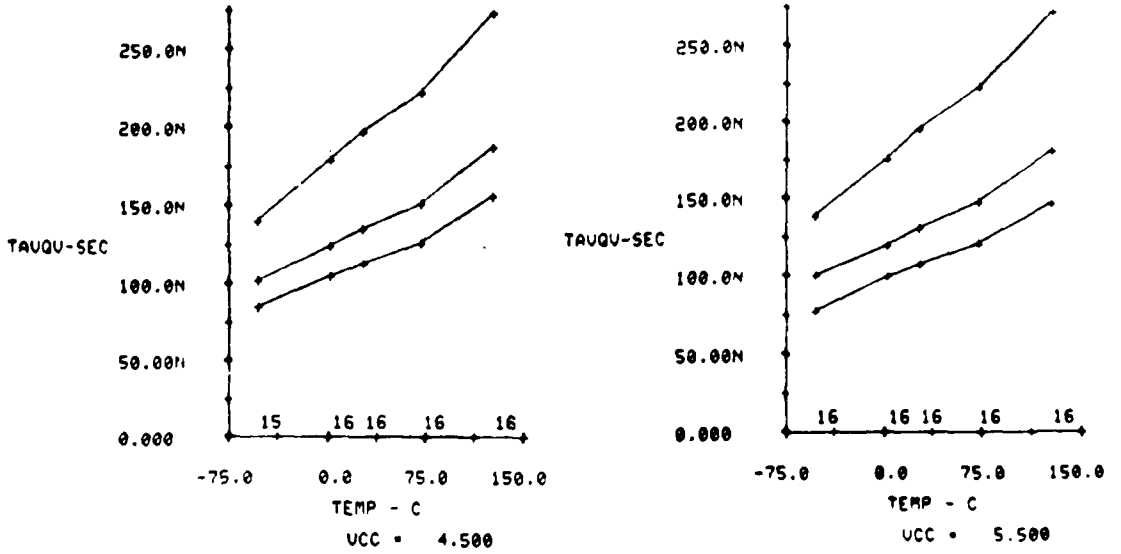



Figure 4.13 Vendor B - Min, Avg, Max Address Access Time Vs. Temperature

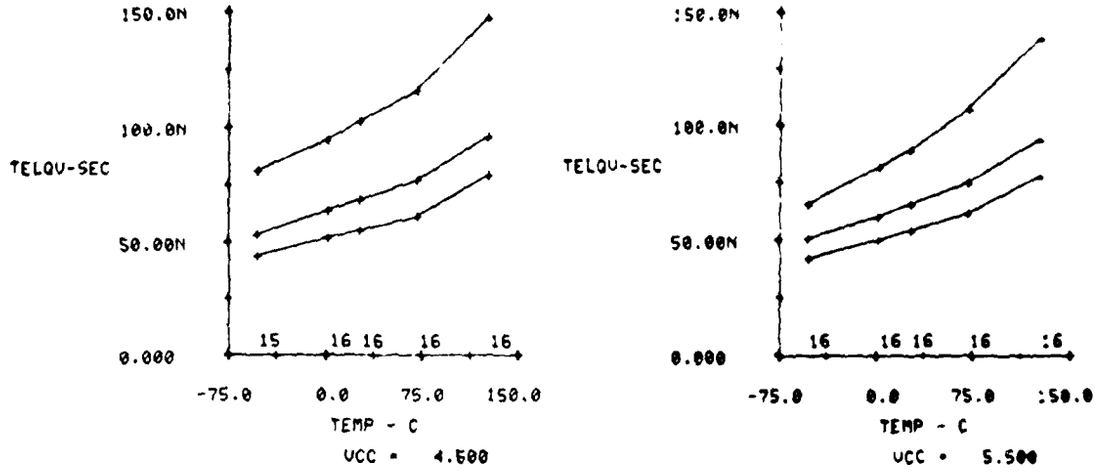



Figure 4.14 Vendor B - Min, Avg, Max Chip Enable Access Time vs. Temperature

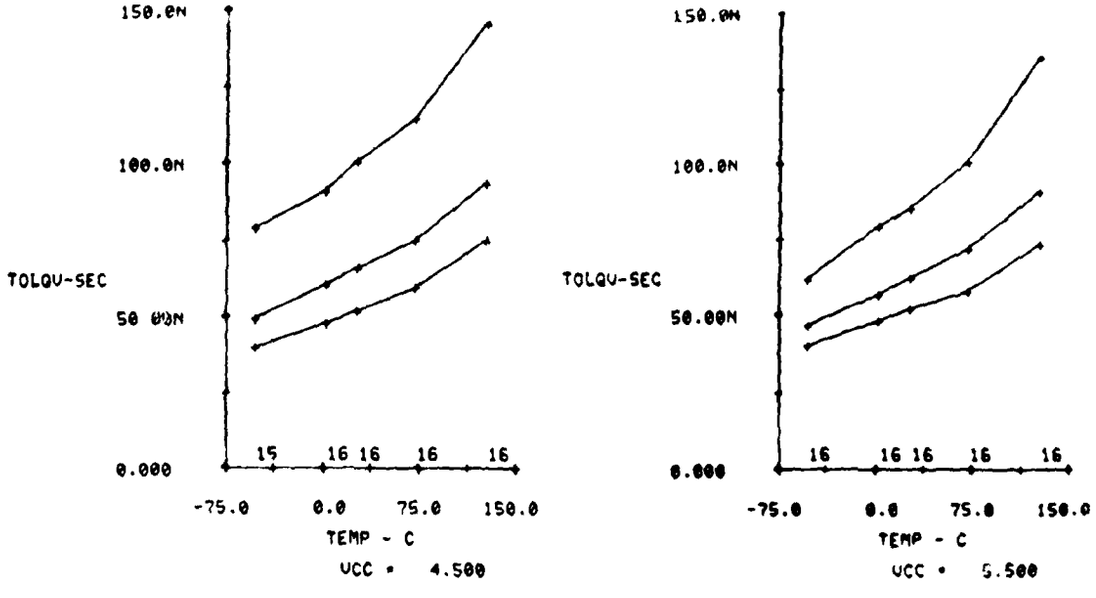



Figure 4.15 Vendor B - Min, Avg, Max Output Enable Access Time vs. Temperature

operate well within the 450ns limits. This data was taken at $V_{IH}$ and $V_{IL}$ levels of 3.0V and 0.4V. As the input logic level sensitivity discussion related, little shift occurs in access times when 2.0V and 0.8V logic levels are used.

4.3.3.2 Other AC Characteristics

Except for the few failures at the temperature extremes, the remaining AC parameters had an unusually large margin between actual values and the specified limits.

The performance of these devices, relative to the limits was discussed with the vendor. However, they elected not to "tighten up" the specification at that time, possibly since a redesign was already planned.

4.3.4 Vendor C

This device type was the only domestically produced 16Kx1 part available and has the highest speed of the four types that were characterized. At the time of the characterization a military version was not planned for the near future. However, while this report was being generated, the vendor had modified the plan to introduce a full military part in 1981.

Vendor C is the only one of the four vendors that specifies AC parameters with a 30pF load capacitance. Like Vendors A and D, Vendor C also uses a 1.5V reference. Since a 50pF load and 2.4V and 0.4V references were used during the characterization, access time measurements indicate that the part is slower than vendor data would indicate.

Because chip enable controls the power down mode, chip enable access time includes power up time and is therefore longer than address access time. Figure 4.16 illustrates the chip enable access time versus temperature at $V_{CC}$ = 4.5V and 5.5V. The data is within the vendor limit in the 0° to 70° temperature range and barely exceeds the limit at -55°C with $V_{CC}$ at 5.5V. If the data had been measured using the same load and output reference used by the vendor, the times would no doubt have fallen within the 55ns limit throughout the entire temperature range.

As with chip enable access time, the remaining characteristics show very good performance over the entire military temperature and $V_{CC}$ range. If the four Vendor C parts are representative of the typical parts produced, this device type has a very high potential as a qualified military device.

4.3.5 Vendor D

The two Vendor D devices show good performance relative to the vendor specifications. In general, both parts operate in the commercial

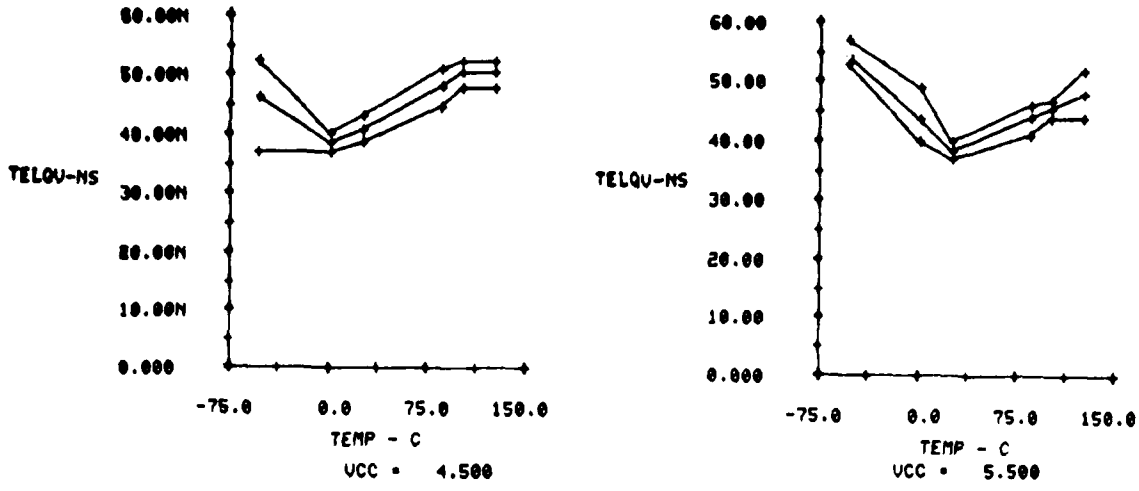



Figure 4.16 Vendor C - Min, Avg, Max Chip Enable Access Time vs. Temperature (4 devices)

temperature range with a comfortable margin between actual values and specified limits.

4.3.5.1 Address, Chip Enable and Output Enable Access Times

Figures 4.17, 4.18, and 4.19 illustrate the access times of the two devices versus temperature. If the parts are "typical" devices, the specified limits for chip enable and output enable access times may have to be increased to allow additional margin at 125°C with $V_{CC}$ = 4.5V. The access times were 69ns as compared to a 70ns limit. Note that chip enable

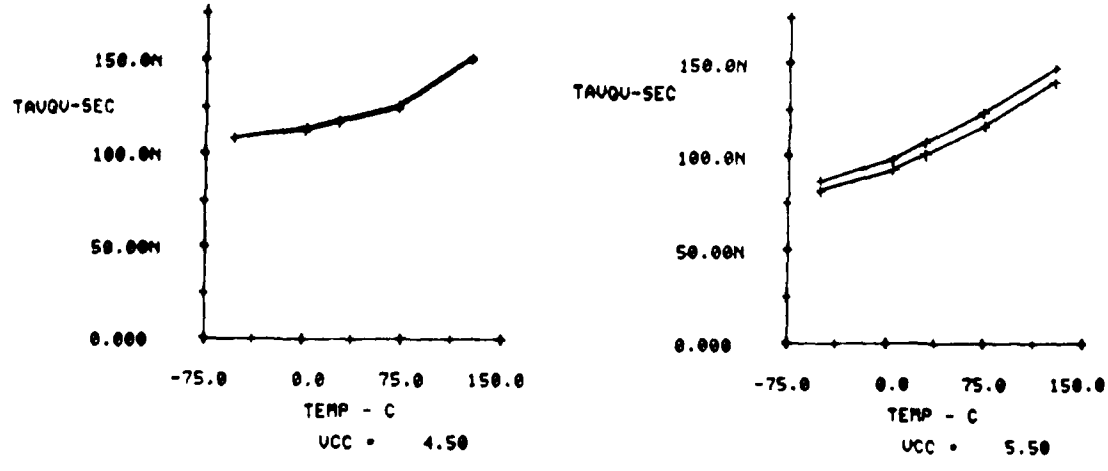



Figure 4.17 Vendor D Address Access Time vs. Temperature (2 devices)

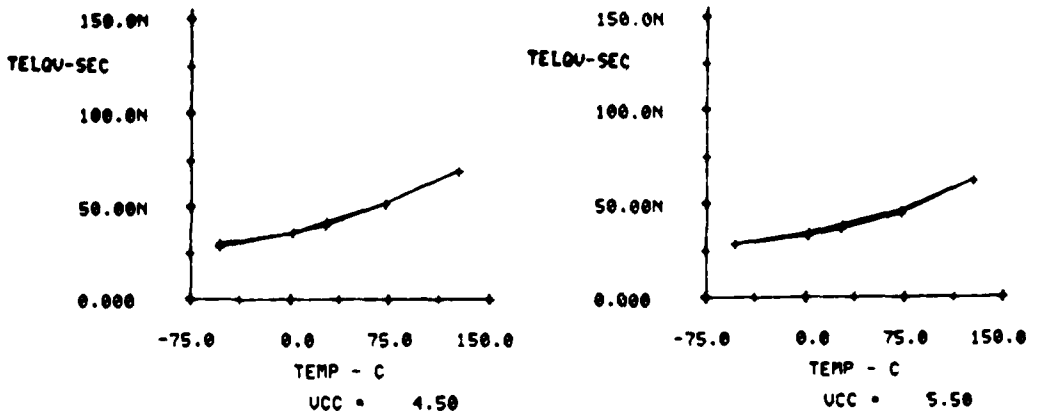



Figure 4.18 Vendor D - Chip Enable Access Time vs. Temperature (2 devices)

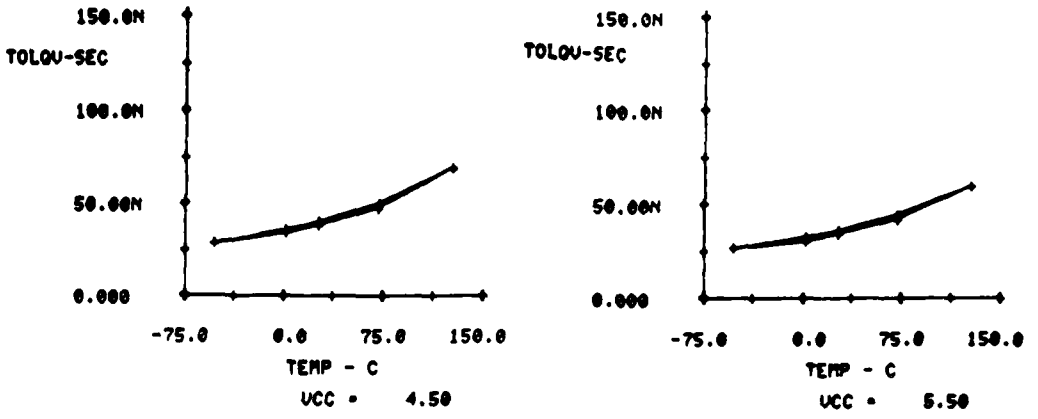



Figure 4.19 Vendor D - Output Enable Access Time vs. Temperature (2 devices)

and output enable access times show little sensitivity to the $V_{CC}$ level.

Chip enable and output enable access times are nearly identical (and specified identically). This suggests that the chip selection function is an ANDing operation of the chip enable and the output enable signals.

4.3.5.2 Address to Data Not Valid (TAXQX)

The data illustrated in Figure 4.20 would indicate that at lower commercial temperatures, the parts fail to meet Vendor D's specified 20ns limit. However, as similiarly indicated for Vendor A, output voltage references used for the measurements, were different than the vendor reference. The vendor uses a 1.5V output reference. This would include significant additional time in the measurement value, for the output to transit from a valid logic level (used as the reference in this characterization) to a 1.5V level.

4.3.5.2 Other AC Parameters

One of the two parts failed three parameters, TWHAX, TDVWL, and TELWH at 125°C with $V_{CC}$ at 5.5V. The limits at all other conditions were easily met. The other device met the limits at all test conditions.

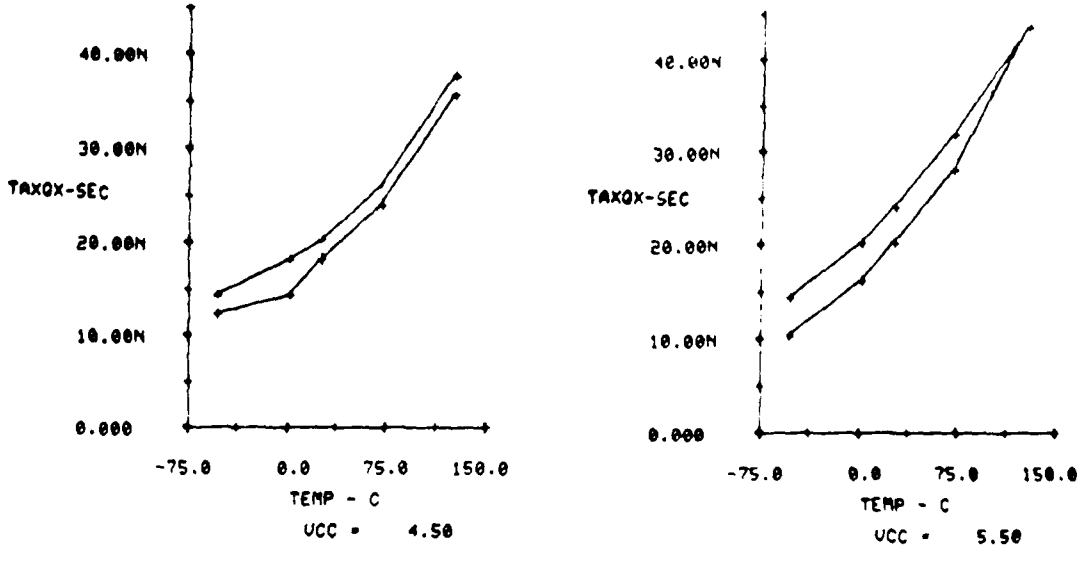



Figure 4.20 Vendor D - Address to Data Not Valid Time vs. Temperature (2 devices)

## 5. SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS

Vendor A exhibited a significant sensitivity to logic high input levels. When the logic high voltage was set to the vendor's specified 2.2V level, performance was poor, even in the commercial temperature range. When the logic high voltage was set to 3.0V, the general performance relative to the vendor limits, was good over the entire military temperature and $V_{CC}$ ranges. At -55°C two of 18 devices failed at higher $V_{CC}$ levels.

Vendor A has undertaken a redesign of the part to eliminate an addressing anomaly that occurred when one or more address bits were delayed from the remaining bits. (The delay was more than a few nanoseconds but less than the minimum cycle time.)

Of 22 Vendor B devices received, six failed the vendor specified limits. The remaining Vendor B devices performed well at all temperatures and $V_{CC}$s throughout the military ranges although some sensitivity was noted at -55°C. Devices that were rejected from the characterization process exhibited a high degree of sensitivity to temperatures below 25°C. The sensitivity was linked to substrate bias voltage instability. It is suspected that those parts not rejected from the characterization that were sensitive to -55° had a similar substrate bias problem but to a much lesser extent.

The characterization data shows that very wide margins exist between device operating limits and vendor specified limits. It is conceivable that the vendor could "tighten up" the specification limits to make the part more appealing without compromising yields. In any case the current specification may be totally irrelevant since the vendor has initiated a redesign of the part to improve performance over the military temperature range.

The four Vendor C parts performed very well under all conditions within and including the military extremes. The sample size was limited, but the parts show high potential as qualified military devices. The vendor plans to introduce a military version in November 1981.

The two Vendor D devices exceeded the supply current at 0°C, but all other characteristics were within vendor commercial limits. One of the two parts failed at $V_{CC}$ = 5.5V with temperature at 125°C.

Vendor D does not plan domestic production of this type. The devices were made available for a general assessment of the technology used in their design. Based on the chip size, specified limits, and overall performance, the design could be described as conservative in nearly all aspects.

Of all four device types addressed in the characterization, no two can be considered interchangeable. One is simply a different configuration, while the other have significantly different operating limits.

Figure 5.1 illustrates the diversity in access time characteristics. The figure represents the average access times,at various temperatures, of the device quantities indicated in parentheses. Other device parameters

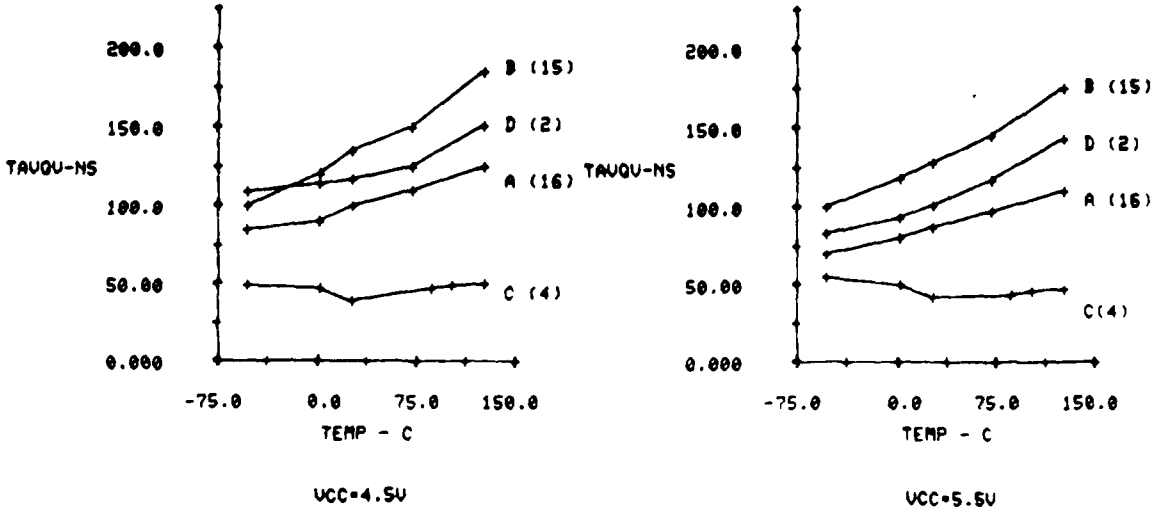



Figure 5.1 All Vendors - Average Access Time vs. Temperature

are similiarly different. In addition Vendor A has a sensitivity to logic high input voltage, which makes it undesireable in an environment that requires a noise margin. (Vendor A recently published a specification for a military version of this part that uses 2.4V for a $V_{IH}$ limit.)

As part of future comprehensive characterization effort it is recommended that specifications for the redesigned Vendor A and Vendor B parts be reviewed. If they show promise as military parts, quantities should be procurred and evaluated to assess operating limits as well as to determine whether new and old sensitivities exist.

Future effort should also include procurement and full characterization of military devices from Vendor C. The speed and power down mode of this device make it an attractive part for many applications.

If available, other 16K static RAM types should be evaluated for military use. As more device types become available the possibility of interchangeable parts improves.

Relative to all memory types and other digital devices with high impedance outputs, further investigation is needed to develop an output disable time measurement technique for automatic test equipment. The measurement must eliminate the effects of external capacitance while avoiding conditions that would damage a device output.

# 6. APPENDIX

## FUNCTIONAL ALGORITHMS

The functional algorithms herein describe the address, data, read and write sequences performed on the memory devices during the AC characterization and test pattern sensitivity studies.

## Marching 1/0 Pattern

This pattern is used to test for bit independence and address uniqueness. A variation of the pattern is also used to check that data cannot be written into the device when it is deselected. The basic March pattern is performed in the following sequence:

Step 1 - Write the array with background data.
Step 2 - Read the entire memory for background data.
Step 3 - Read address location zero for background data.
Step 4 - Write address location zero with complement data.
Step 5 - Read address location zero for complement data.
Step 6 - Repeat steps 3 through 5 for each address location.
Step 7 - Repeat steps 3 through 6 using complement data and addresses the decrement from maximum.
Step 8 - Repeat Steps 3 through 7 with complement data.

When verifying that data cannot be written while the chip is deselected, the pattern is performed in the following sequence:

Step 1 - Write the array with background data.
Step 2 - Read the entire memory for background data.
Step 3 - Read address location zero for background data.
Step 4 - Deselect the device and attempt to write complement data at location zero.
Step 5 - Read address location to verify that complement data was not written into location zero.
Step 6 - Repeat steps 3 through 5 for all addresses.
Step 7 - Repeat steps 1 through 7 with complement data.

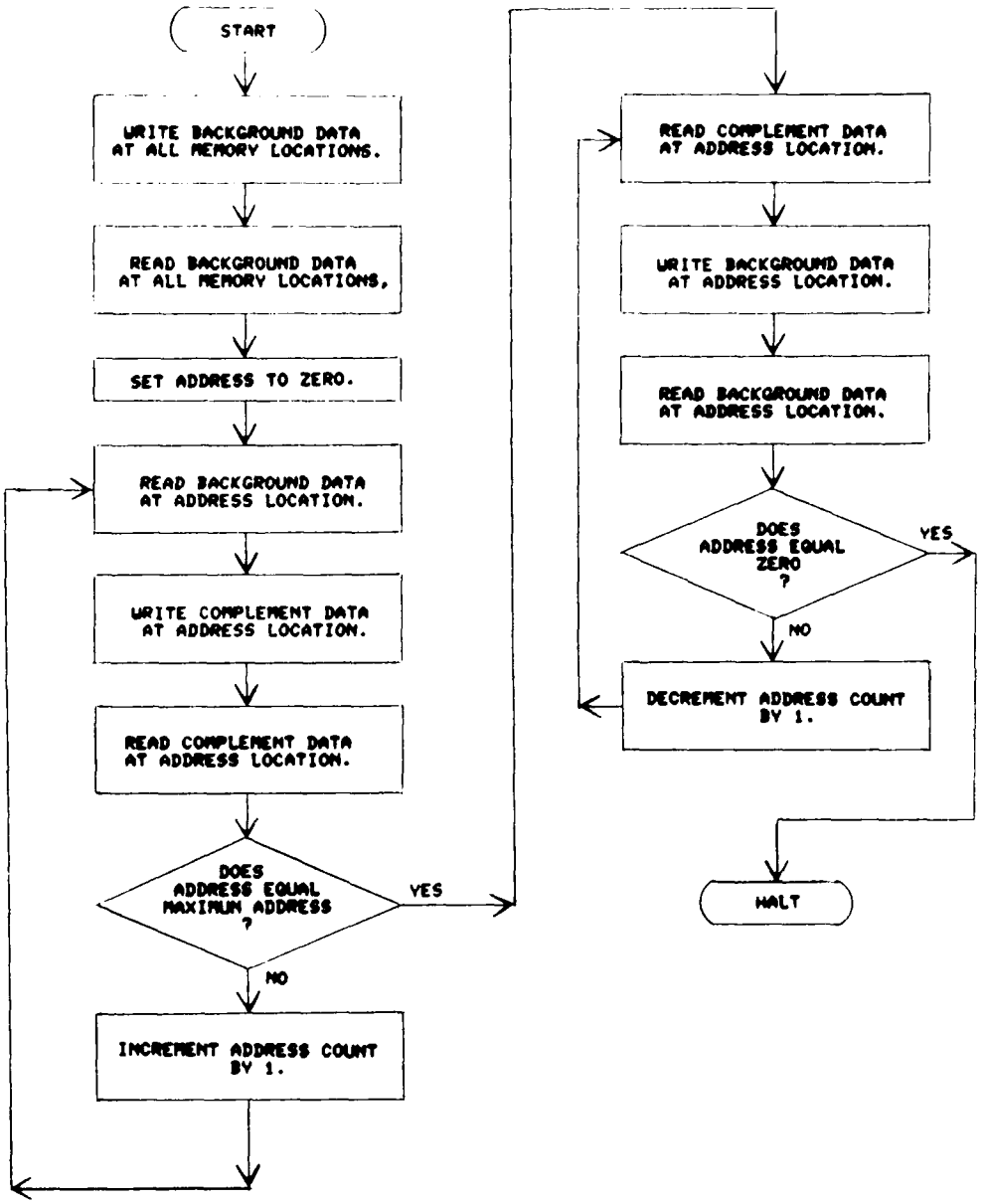



Figure 6.1 Marching Pattern Flowchart

## Galloping Address Pattern

This pattern is used to check memory access time between one address and every other address. It is performed in the following manner:

Step 1 - Write a background pattern throughout the memory.
Step 2 - Read the array for background pattern.
Step 3 - Write the complement data at the first address location (test location).
Step 4 - Read address locations in sequence:
read test location (address 1), read location 2, read test location, read address location 3, read test location.
Read in sequence until every address location within the array is read.
Step 5 - Write test location with background data.
Step 6 - Select the second location as the address location and repeat sequence in steps 3 through 5.
Step 7 - Repeat steps 3 through 5 until each cell within the array is used as the test location.
Step 8 - Repeat steps 1 through 8 with complement data.

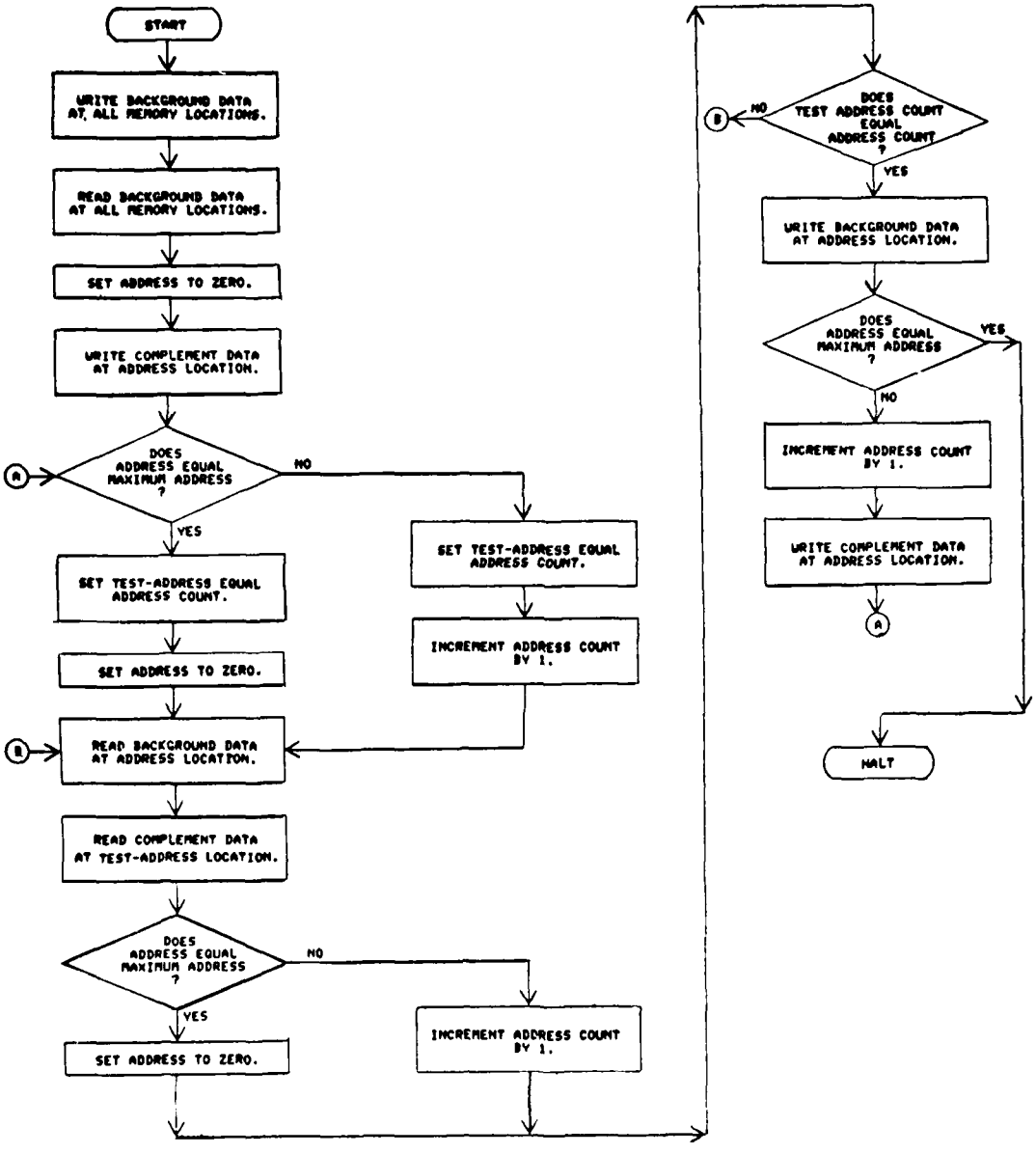



Figure 6.2 Galloping Pattern Flowchart

## Galloping Row Pattern

This pattern is used to check memory access time between one row address in a column and every other row address in the same column. The pattern is performed in the following sequence:

Step 1 - Write a background pattern throughout the memory.
Step 2 - Read the array for the background pattern.
Step 3 - At the first column address write complement data into the first row address (test row).
Step 4 - Read row addresses in this sequence: read test row (row 1), read row 2, read test row, read row 3, read test row. Read in this sequence until every row address in that column address has been read.
Step 5 - Write the background data into the test row.
Step 6 - Select the second row as the test row and repeat steps 3 through 5.
Step 7 - Repeat steps 3 through 6 until all rows at that column address have been used as test rows.
Step 8 - Repeat steps 3 through 7 at the remaining column addresses.

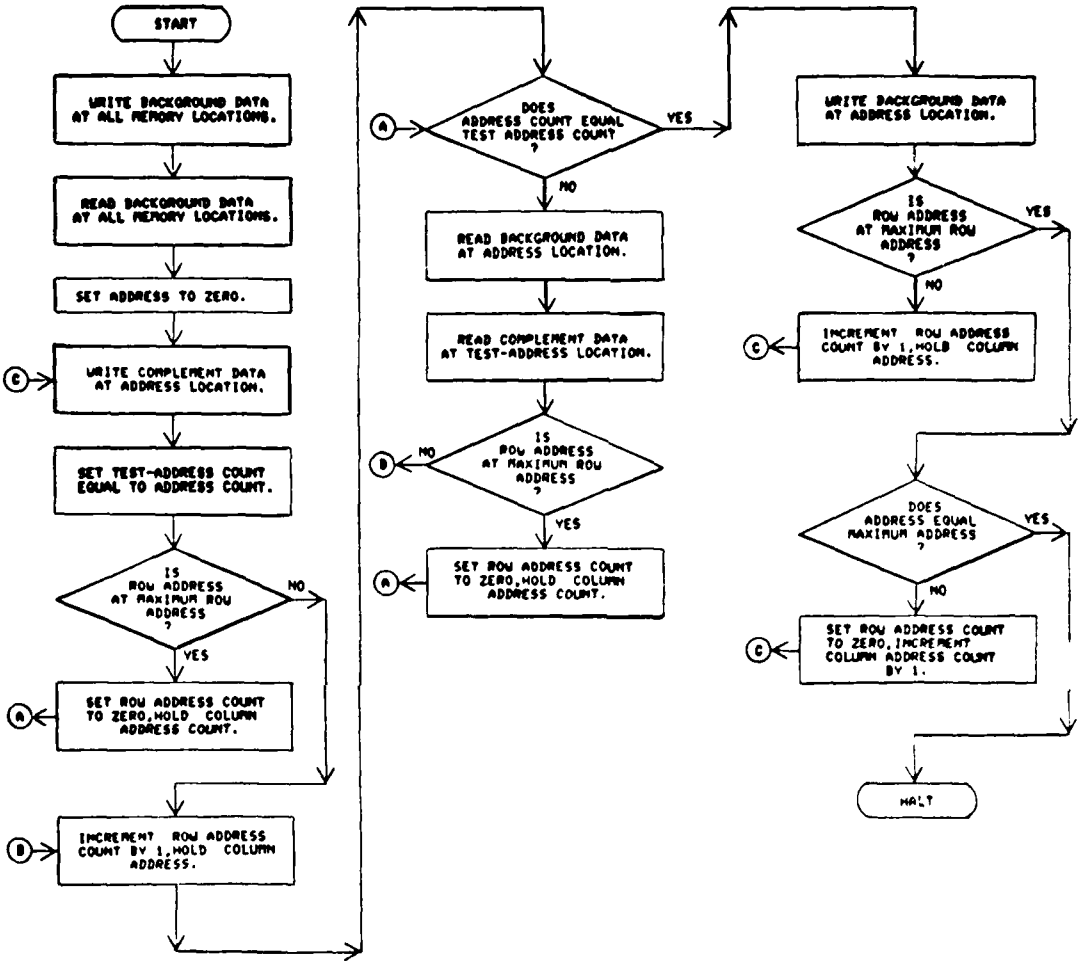



Figure 6.3 Galloping Row Pattern Flowchart

Galloping Column Pattern

This pattern is used to check memory access time between one column address in a row and every other column address in the same row. The pattern is performed in the following sequence:

Step 1 - Write a background pattern throughout the memory.
Step 2 - Read the array for the background pattern.
Step 3 - At the first row address, write complement data into the first column address (test column).
Step 4 - Read column addresses in this sequence: read test column (column 1), read column 2, read test column, read column 3, read test column. Read in this sequence until every column at that row address has been read.
Step 5 - Write the background data into the test column.
Step 6 - Select the second column as the test column and repeat steps 3 through 5.
Step 7 - Repeat steps 3 through 6 until all columns at that row address have been used as test columns.
Step 8 - Repeat steps 3 through 7 at the remaining row addresses.

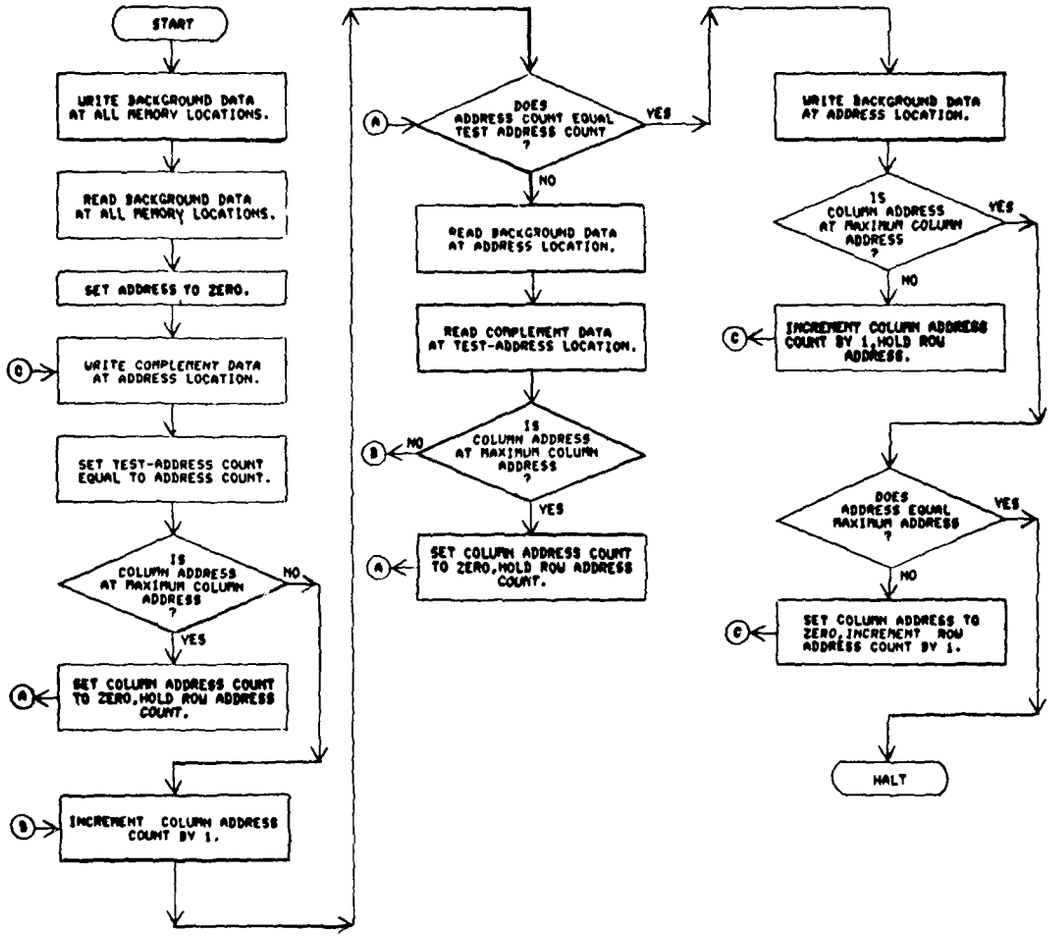



Figure 6.4 Galloping Column Pattern Flowchart

## Inter-Address Write Recovery

This pattern is used to check transitions from a Write at one address to a Read at another address. The pattern is performed in the following manner:

Step 1 - Write the entire array with background data.
Step 2 - Read the entire array for background data.
Step 3 - Select address location zero as the test-address.
Step 4 - Write complement data at address location 1.
Step 5 - Read the test-address location for background data.
Step 6 - Read the address location 1 for complement data.
Step 7 - Write background data at address location 1.
Step 8 - Read the test-address location for background data.
Step 9 - Read the address location 1 for background data.
Step 10 - Repeat steps 4 through 9 for every address in the array.
Step 11 - Repeat steps 3 through 10 until each address has been the test address.
Step 12 - Repeat steps 1 through 11 with complement data.

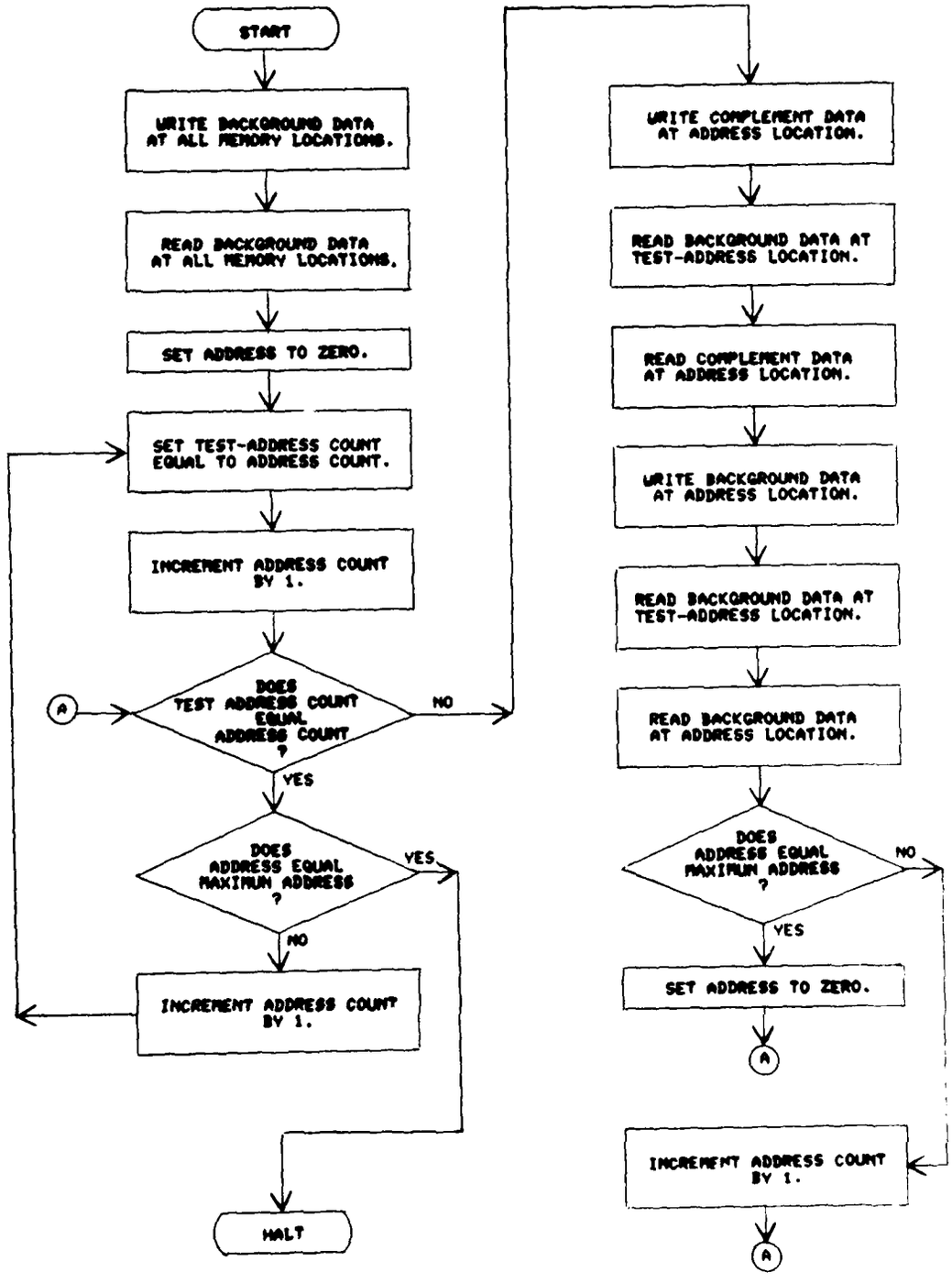



Figure 6.5 Inter-Address Write Recovery Flowchart

## Inter-Row Write Recovery

Step 1 - Write the entire array with background data.
Step 2 - Read the entire array for background data.
Step 3 - Set the first row address location of the first column as the test-address.
Step 4 - Write complement data at the second row address of the first column.
Step 5 - Read the test-address location for background data.
Step 6 - Read the second row address location of the first column for complement data.
Step 7 - Write the second row address location of the first column with background data.
Step 8 - Read the test-address location for background data.
Step 9 - Read the second row address location of the first column for background data.
Step 10 - Repeat steps 4 through 9 for each row address within that column.
Step 11 - Repeat steps 3 through 10 until each row in that column has been the test row.
Step 12 - Repeat steps 3 through 11 for each column.
Step 13 - Repeat steps 1 through 12 with complement data.

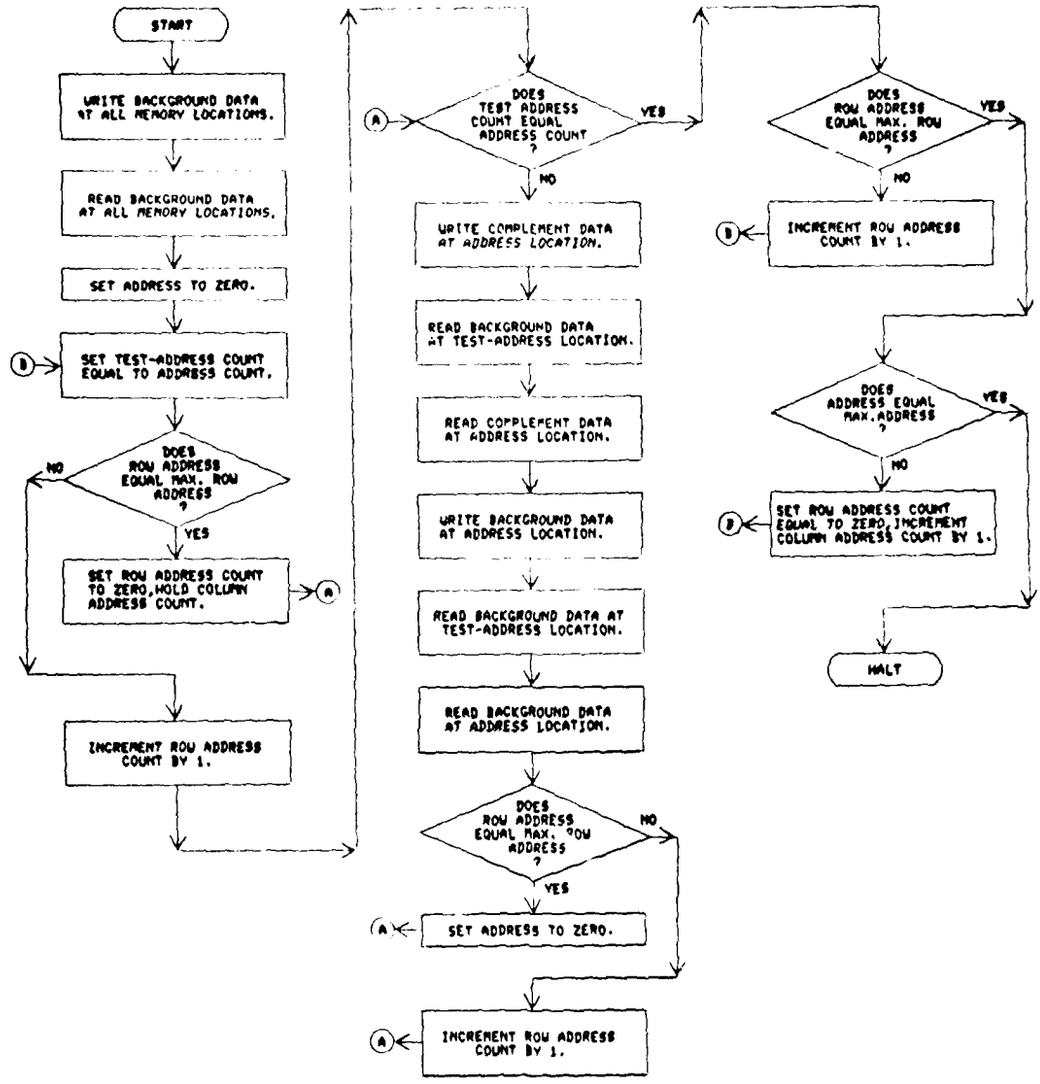



Figure 6.6 Inter-Row Write Recovery Pattern Flowchart

Inter-Column Write Recovery

Step 1 - Write the entire array with background data.
Step 2 - Read the entire array for background data.
Step 3 - Set the first column address location of the first row as the test-address.
Step 4 - Write complement data at the second column address of the first row.
Step 5 - Read the test-address location for background data.
Step 6 - Read the second column address location of the first row for complement data.
Step 7 - Write the second column address location of the first row with background data.
Step 8 - Read the test-address location for background data.
Step 9 - Read the second column address location of the first row for background data.
Step 10 - Repeat steps 4 through 9 for each column address within that row.
Step 11 - Repeat steps 3 through 10 until each column in that row has been the test column.
Step 12 - Repeat steps 3 through 11 for each row.
Step 13 - Repeat steps 1 through 12 with complement.

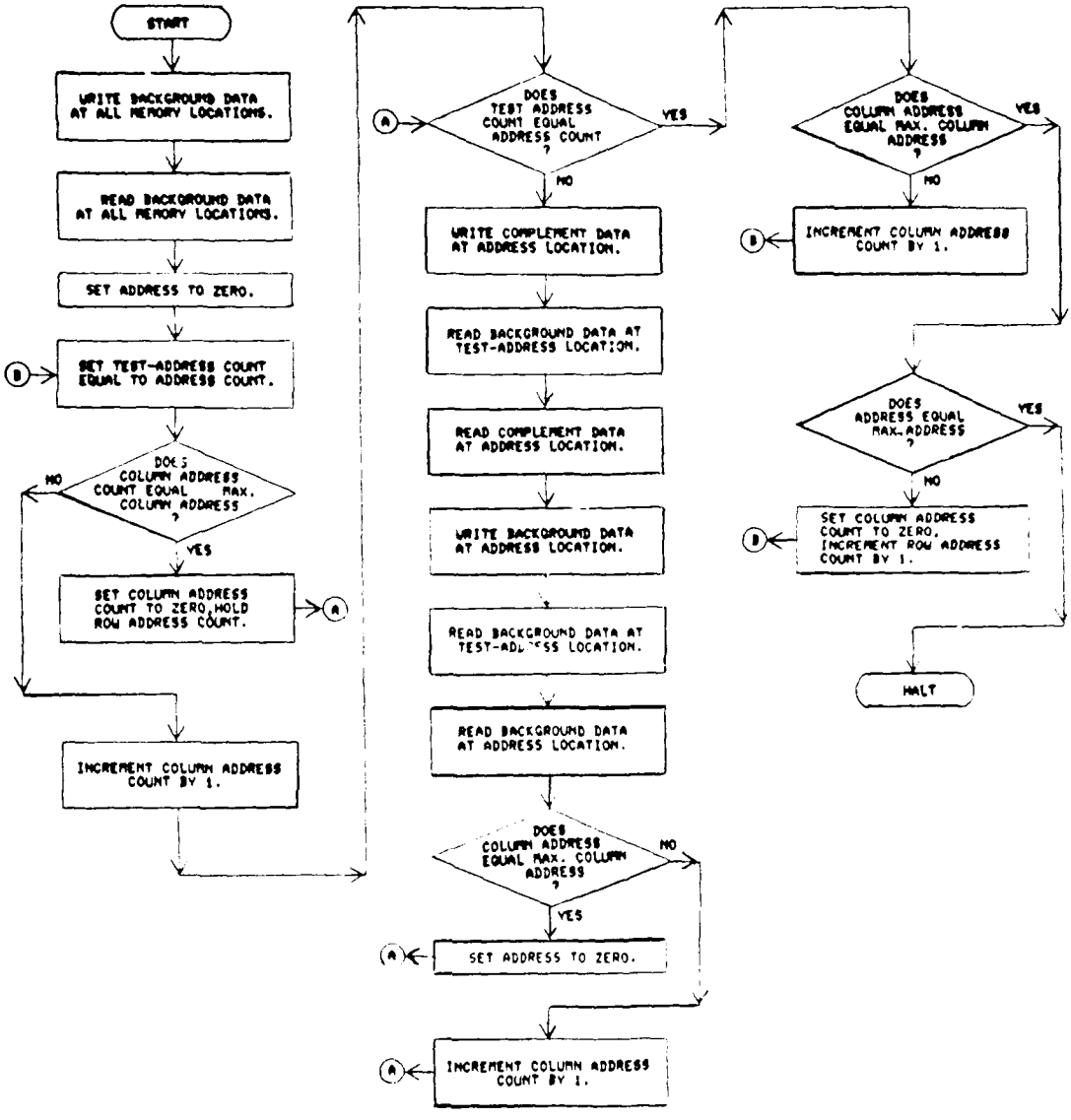



Figure 6.7 Inter-Column Write Recovery Flowchart

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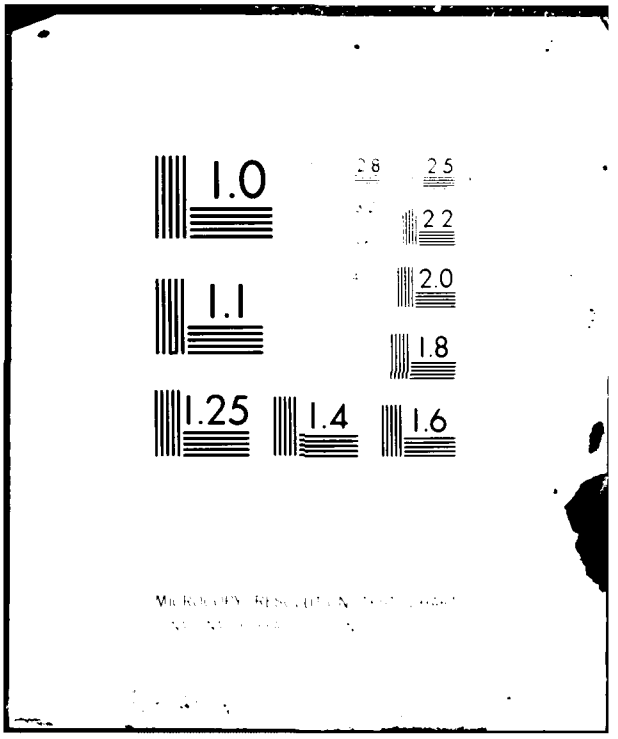
1.0
2.8
2.5
2.2
1.1
2.0
1.8
1.25
1.4
1.6

## Read/Write Address Complement Pattern

Step 1 - Write 1s and 0s alternately into the array.
Step 2 - Read 1s at address location zero.
Step 3 - Write 0s at address location zero.
Step 4 - Read 0s at complement address location.
Step 5 - Write 1s at this address location.
Step 6 - Read 0s at address location one.
Step 7 - Write 1s at address location one.
Step 8 - Read 1s at the complement address location.
Step 9 - Write 0s at this address location.
Step 10 - Repeat steps 2 through 9 until finished with every address in the array.
Step 11 - Read out data pattern from memory.
Step 12 - Repeat steps 1 through 11 with complement data.

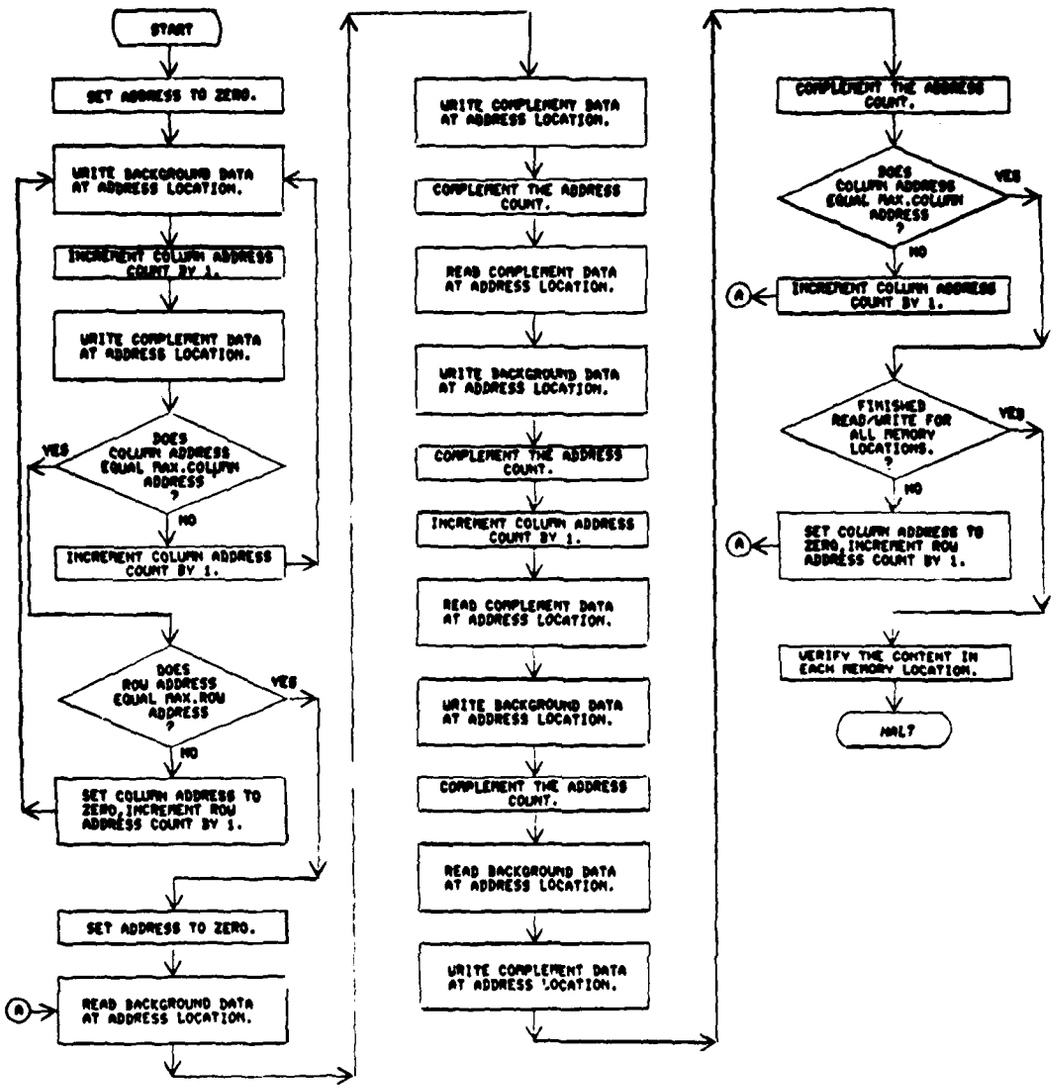


Figure 6.8 Read/Write Address Complement Pattern Flowchart

## Read/Write Row Complement Pattern

Step 1 - Write 1s and 0s alternately within each column.
Step 2 - Read 1s at the first row address in the first column.
Step 3 - Write 0s at the same location.
Step 4 - Read 0s at the complement row address location in the same column.
Step 5 - Write 1s at this complement row address location.
Step 6 - Read 0s at the second row address location.
Step 7 - Write 1s at the second row address location.
Step 8 - Read 1s at the complement-second-row address location.
Step 9 - Write 0s at this complement-second-row address location.
Step 10 - Repeat steps 2 through 9 until finished with every row address in that column.
Step 11 - Repeat steps 2 through 10 for the remaining columns.
Step 12 - Read out data pattern from memory.
Step 13 - Repeat steps 1 through 12 with complement data.

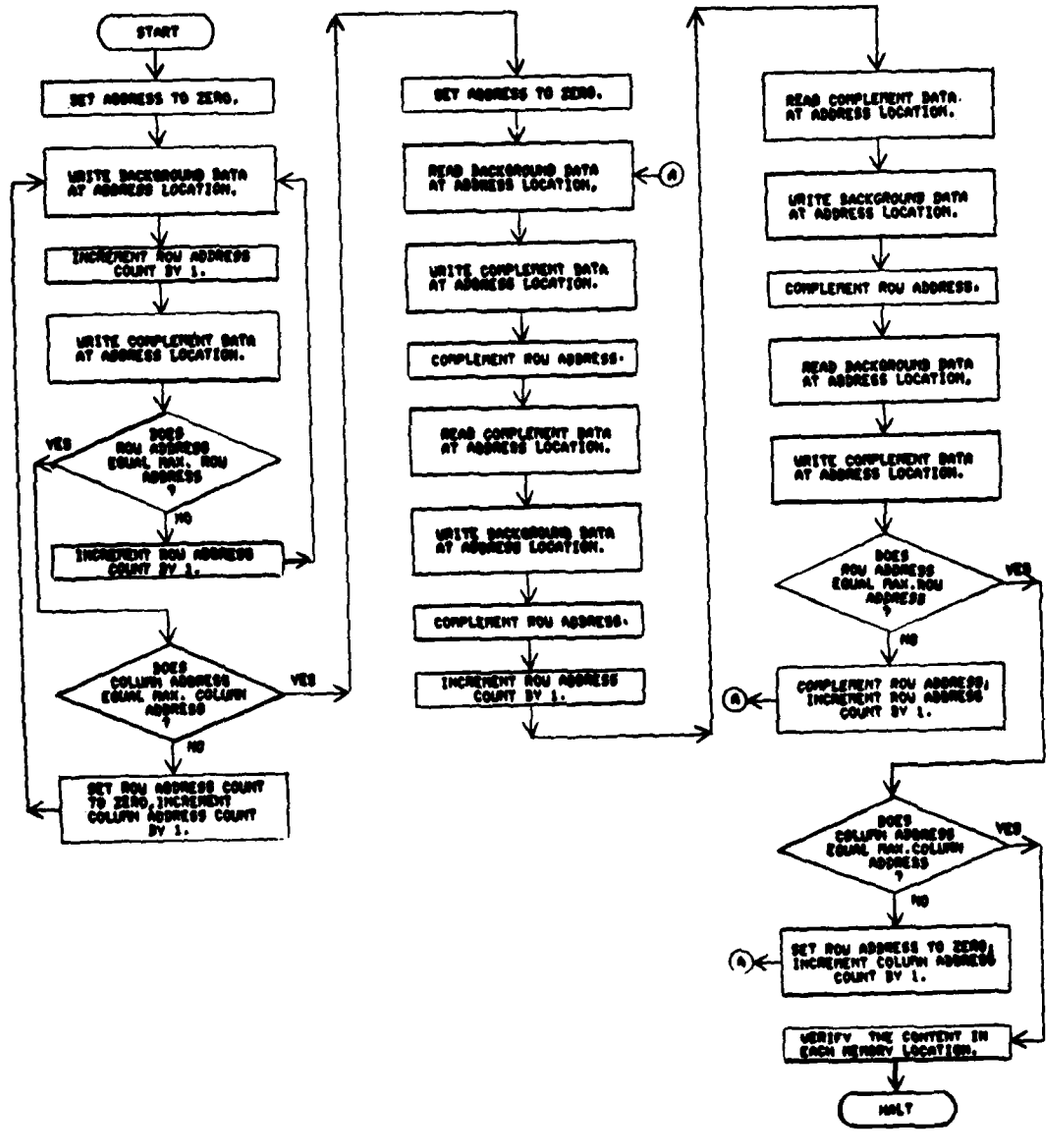


Figure 6.9 Read/Write Row Complement Pattern Flowchart

Read/Write Column Complement (RWCLAD) Pattern

Step 1 - Write 1s and 0s alternately within each row.
Step 2 - Read 1s at the first column address in the first row.
Step 3 - Write 0s at the same location.
Step 4 - Read 0s at the complement column address location in the same row.
Step 5 - Write 1s at this complement column address location.
Step 6 - Read 0s at the second column address location.
Step 7 - Write 1s at the second column address location.
Step 8 - Read 1s at the complement-second-column address location.
Step 9 - Write 0s at this complement-second-column address location.
Step 10 - Repeat steps 2 through 9 until finished with every column-address in that row.
Step 11 - Repeat steps 2 through 10 for the remaining rows.
Step 12 - Read out data pattern from memory.
Step 13 - Repeat steps 1 through 12 with complement data.

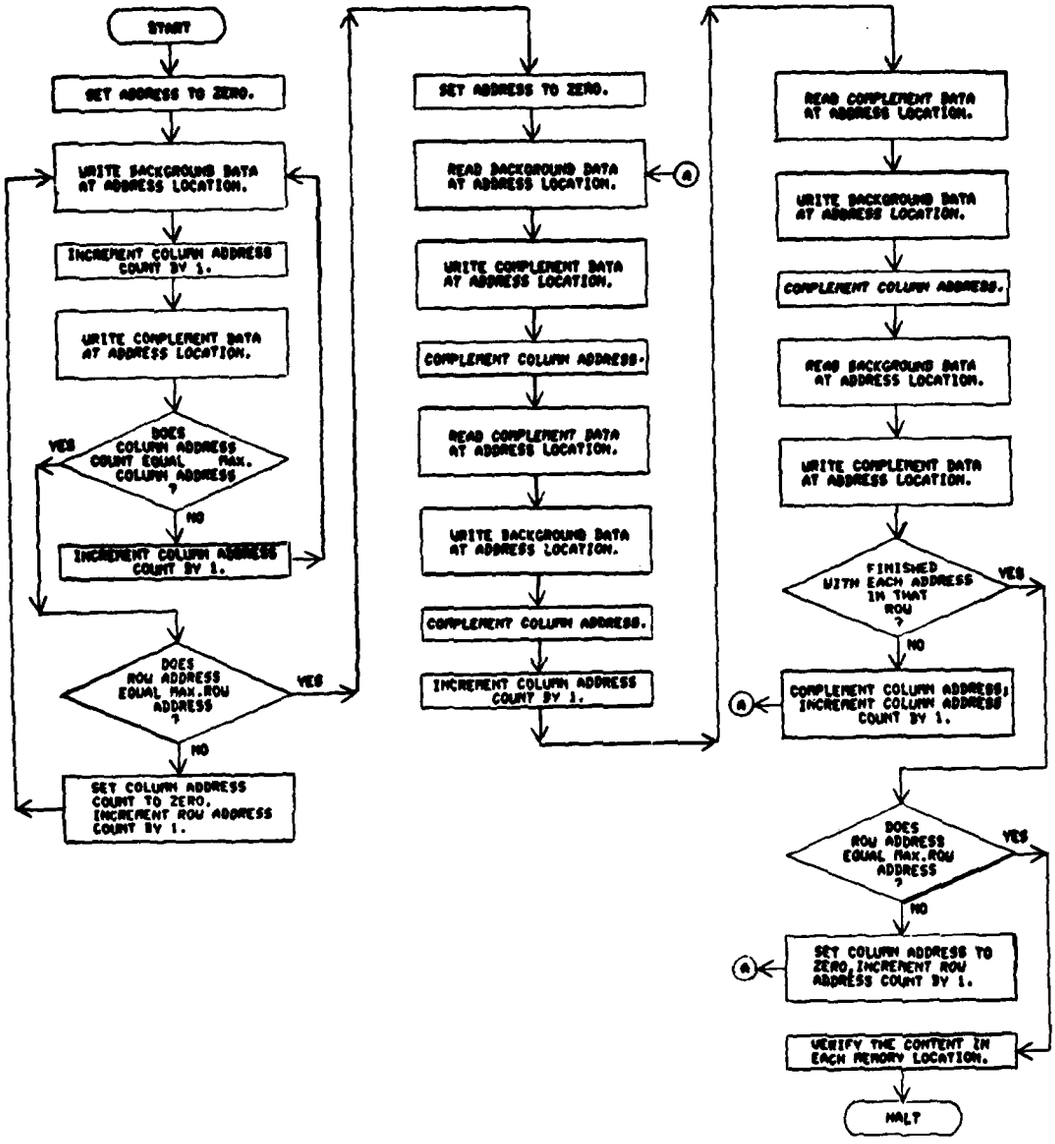


Figure 6.10 Read/Write Column Complement Pattern Flowchart

## Write/Write Address Complement

Step 1 - Write 1s at the minimum address location.
Step 2 - Write 0s at the maximum address location.
Step 3 - Write 0s at the minimum +1 address location.
Step 4 - Write 1s at the maximum -1 address location.
Step 5 - Continue steps 1 through 4 incrementing and decrementing from minimum and maximum address locations until all locations have been written with data.
Step 6 - Repeat steps 1 through 5 by replacing write with read.
Step 7 - Repeat steps 1 through 6 with opposite data.

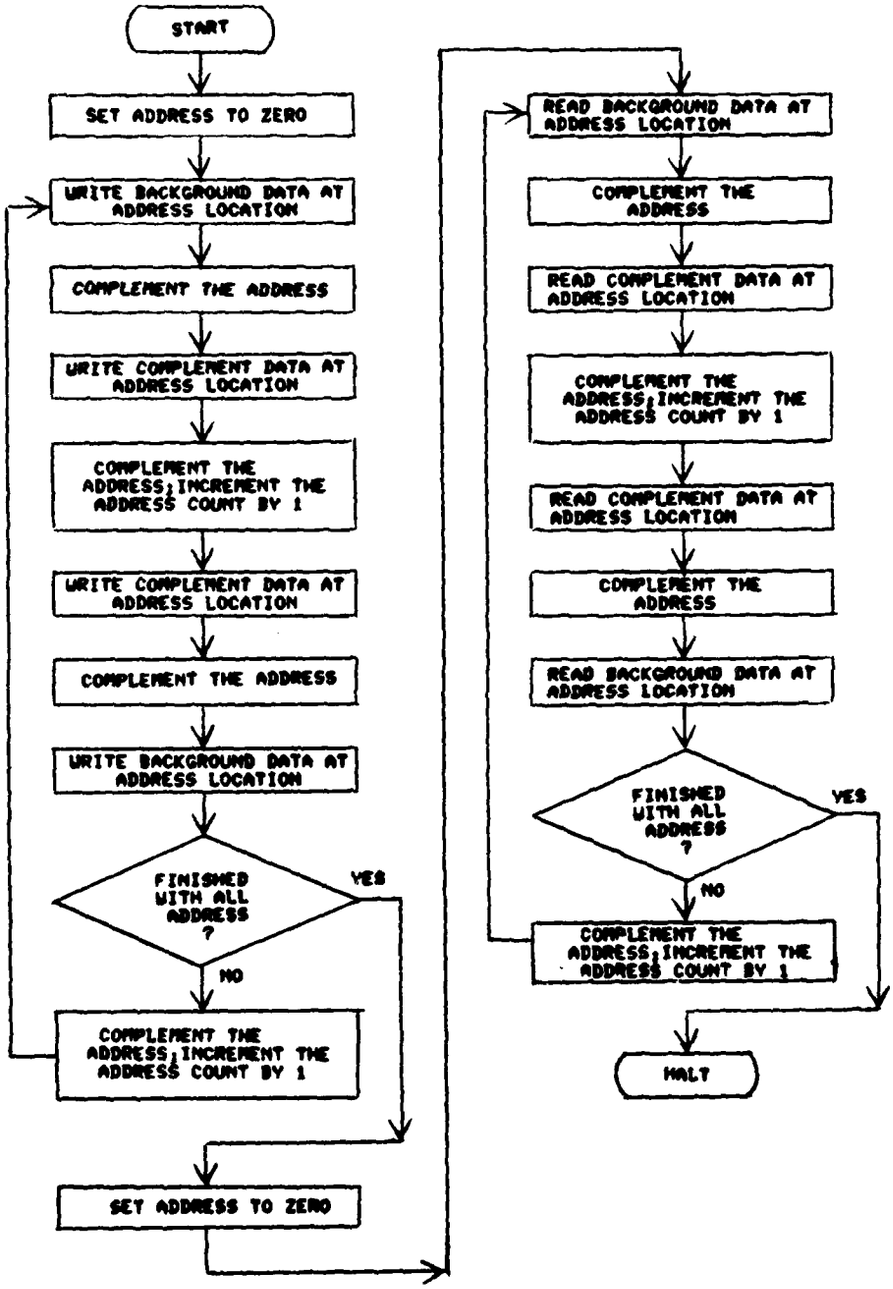


Figure 6.11 Write/Write Address Complement Flowchart

## Write/Write Row Complement

The WWROAD is performed in the following manner:

Step 1 - Write 1s at the minimum row address location of the first column.
Step 2 - Write 0s at the maximum row address location of the first column.
Step 3 - Write 0s at the minimum +1 row address location of the first column.
Step 4 - Write 1s at the maximum -1 row address location of the first column.
Step 5 - Continue steps 1 through 4 incrementing and decrementing from minimum and maximum row address locations until all row address locations have been written with data.
Step 6 - Repeat steps 1 through 5 for each column of the array.
Step 7 - Repeat steps 1 through 6 by replacing write with read.
Step 8 - Repeat steps 1 through 7 with opposite data.

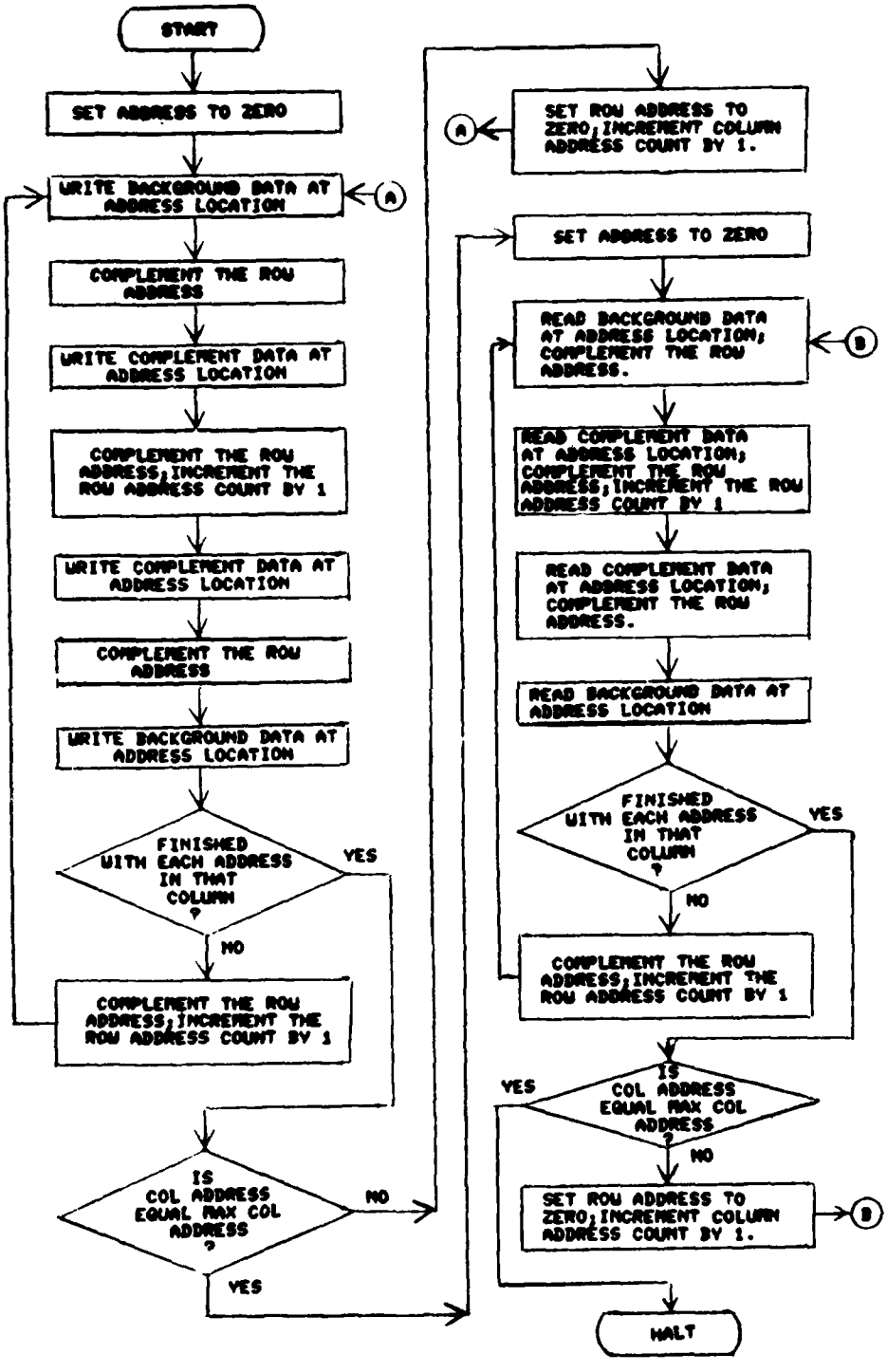


Figure 6.12 Write/Write Row Complement Pattern Flowchart

## Write/Write Column Complement

The WWCLAD is performed in the following sequence:

Step 1 - Write 1s at the minimum column address location of the first row.
Step 2 - Write 0s at the maximum column address location of the row.
Step 3 - Write 0s at the minimum +1 column address location of the first row.
Step 4 - Write 1s at the maximum -1 column address location of the first row.
Step 5 - Continue steps 1 through 4 incrementing and decrementing from minimum and maximum column address locations until all column address locations have been written with data.
Step 6 - Repeat steps 1 through 5 for each row of the array.
Step 7 - Repeat steps 1 through 6 by replacing write with read.
Step 8 - Repeat steps 1 through 7 with opposite data.

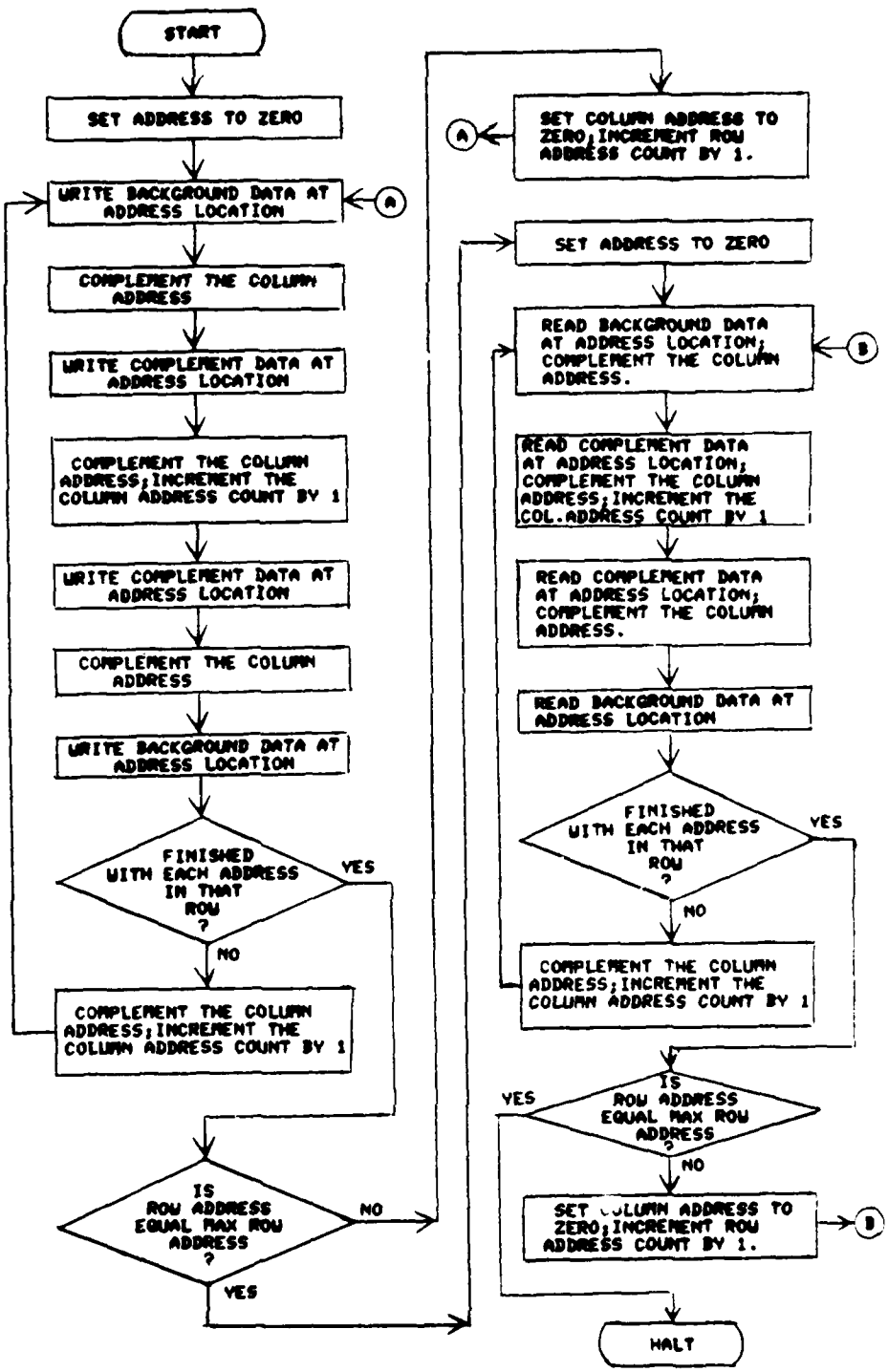


Figure 6.13 Write/Write Column Complement Pattern Flowchart

## Sliding Diagonal Pattern

The sliding diagonal pattern checks sense amplifiers and address decoders of the memory by utilizing a diagonal addressing scheme to perform read and write operations on the DUT. A test diagonal of complement data is first written into the array against background data. The memory is then read diagonally verifying background and test data. The test diagonal is then restored with background data and the next adjacent diagonal becomes the test diagonal. This procedure is repeated until all diagonals have been exercised as the test diagonal and again for the complement data. The pattern is performed in the following sequence:

Step 1 - Write the array with background data.
Step 2 - Read the entire memory for background data.
Step 3 - Write a test diagonal with complement data.
Step 4 - Diagonally read background data at all other diagonals.
Step 5 - Read the test diagonal for complement data.
Step 6 - Restore the test diagonal with background data, and write the next test diagonal at one of the adjacent diagonals.
Step 7 - Repeat steps 4 through 6 until all diagonals have been exercised as the test diagonal.
Step 8 - Repeat steps 1 through 7 with complement data.

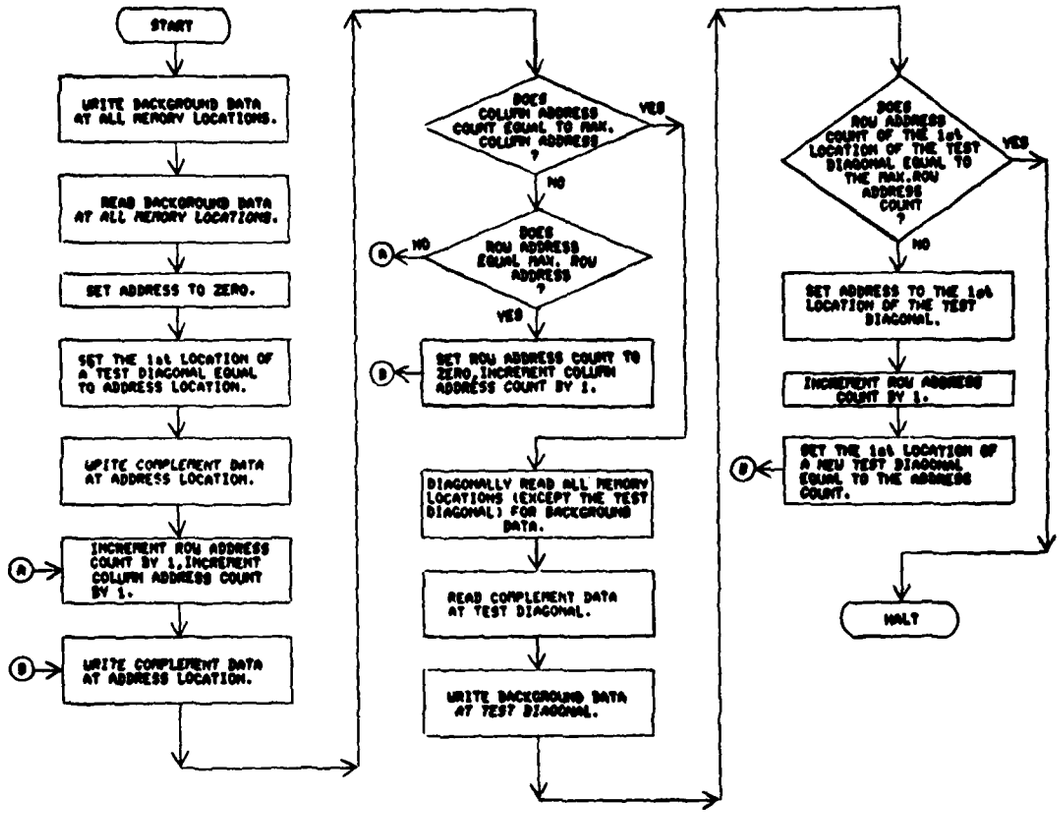


Figure 6.14 Sliding Diagonal Pattern Flowchart

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